SOI-Enabled MEMS Processes Lead to Novel Mechanical, Optical, and Atomic Physics Devices

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Abstract- **Beginning in the mid-1990s, Sandia National Laboratories began its migration to Silicon-on-Insulator (SOI) wafers to develop a radiation-hardened semiconductor process for sub-0.5μm geometries. Successfully radiation hardening SOI technologies enabled an in-house processing familiarity that exceeded our expectations by opening opportunities to improve other technologies. Rather than rely on a single SOI technology, we have developed families of SOI processes using SOI wafers specifically tailored for each of a number of diverse applications.**

From this SOI expertise, we have designed, developed, and fabricated a number of novel devices that exploit a variety of mechanical, electrical, and optical phenomena, including atomic-physics based devices. We present a high-level description of our SOI process technologies using product examples. Of particular note are a novel accelerometer, RF MEMS microresonators and contacting switches, integrated optics (low-loss Si waveguides, the smallest and lowest power micro-ring modulators and thermo-optic phase modulators/switches), and ion traps for quantum computing (along with other atomic physics device examples).

I. INTRODUCTION

Silicon on Insulator (SOI) technologies have long been of interest for high-performance integrated circuits due to their reduced parasitic capacitance for high frequency operation as well as their ability to protect active transistors from substrate-generated photocurrents in radiation environments. Thin-film SOI technologies respond to radiation environments somewhat differently than their bulk silicon counterparts due to the presence of the buried oxide underneath the active device. Sandia National Laboratories developed the Body-Under-Source FET (the BUSFET) [1] to achieve the benefits of photocurrent suppression while remaining resistant to total ionizing dose effects. Sandia's SOI work began in the mid-1990s with techniques to characterize and qualify SOI material [2] and extended to the development of a robust BUSFET-based SOI integrated-circuit technology [3].

During roughly the same period, Sandia was also developing a multi-level sacrificial surface micromachining technology for fabricating Micro-Electro-Mechanical Systems, or MEMS [4]. The synergy of developing both a MEMS technology and an SOI integrated-circuit technology in the same fabrication facility on the same equipment soon led to investigations of the possibilities that silicon-on-insulator wafers could provide for fabricating other novel devices in emerging technologies.

Much of Sandia's success in developing novel SOI-based technologies arises from the unique configuration of Sandia's Microelectronics Development Laboratory (MDL) and its successor the Microsystems Engineering and Sciences Application (MESA) Fabrication facility. These facilities are designed with separately supplied cleanroom bays that allow processing in one bay to proceed without contaminating processes being pursued in adjacent bays. Thus, Sandia was able to develop its earliest MEMS technologies using KOH for anisotropic bulk micromachining in one bay without poisoning the fabrication of sub 0.5-μm-geometry silicon CMOS integrated circuit technologies in adjacent bays. Given this unique flexibility of a research and development microfabrication facility combined with production-worthy standard industrial silicon-processing tools, it is no surprise that Sandia was able to find new uses for the processing flexibility provided by silicon-on-insulator wafers. For our applications, silicon-on-insulator wafers provide structural and processing options impossible with bulk silicon wafers.

Silicon-on-insulator technologies provide high-quality, single-crystalline silicon layers over a buried oxide layer (BOX) of high-quality silicon dioxide which can be exploited for device processing options. The chemical differences between silicon and silicon dioxide enable the use of selective etch processes to remove either layer without disturbing the other. Bosch etching is highly successful in fabricating single crystal bulk-like SOI devices with much thicker SOI layers than the surface silicon layers common in integrated-circuit applications. This usefulness arises from the significant etch selectivity between Si and the BOX. The selectivity is often > 200:1 based on the quality of the oxide and the Si etch rate which is dependent on the aspect ratio of the structure as well as the density of the structures. Etches that selectively attack the buried oxide layer also can be used to lift off the high-quality silicon layer after device processing for flexible, thin membranes containing active devices. Alternatively, the buried silicon dioxide layer can be used as an etch stop for patterning the surface silicon layer, for example, to fabricate radio-frequency MEMS switches with low insertion losses and low propagation losses.

Structurally, the presence of a buried insulator enables the fabrication of high-voltage electronic devices. For optical devices, BOX layer provides a convenient option for silicon channel waveguides using the index difference of the buried layer to contain the optical energy within the

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silicon.

In all these applications, the high-quality silicon surface layer can be chosen with any of a wide range of doping levels and thicknesses for optimization of device performance by tailoring of device structure—independent of whether the devices are optical, mechanical, or electronic. Meanwhile, the poor thermal conductivity of silicon dioxide can be exploited to provide thermal isolation to maximize the impact of temperature excursions on optically based thermal sensors fabricated in the surface silicon layer.

In this paper, we describe these classes of novel devices fabricated at Sandia by exploiting the unique processing and structural options afforded by SOI wafers.

II. Device Technology Examples.

A. Radio-Frequency Devices

The next logical step beyond using SOI wafers for just the high-frequency integrated circuits is to incorporate MEMS switches and resonators on the same circuitry for higher Q filters and RF delay lines without excessive substrate losses.

Sandia has applied the etch selectivity in the silicon-silicon dioxide materials system to fabricate RF MEMS metal contacting switches and RF microresonators, with the intention of adding capability to the existing analog and mixed-signal CMOS SOI electronics. The thermal budgets of these device processes are specifically designed for post-process compatibility with CMOS SOI technology, allowing SOI CMOS active electronics and RF MEMS technologies on a single high-resistivity, low RF loss, silicon substrate.

The RF MEMS switches use low-temperature processing to achieve post-process compatibility with a variety of technologies [5]. The first step in the MEMS switch process is the deposition of a bottom contact metal on top of a silicon nitride layer. Next, PECVD SiO_2/Si/SiO_2 layers are deposited as a sacrificial film. Contact dimples are etched through the first layer of SiO_2 to the Si etch-stop layer, generating a smooth contact dimple with controllable depth. Openings are etched through the entire film stack to provide device anchoring. Then, the switch body is electroplated and the sacrificial layers are removed. These RF MEMS switches typically have insertion loss <0.1 dB and bandwidth >20 GHz, adding a high-linearity, low-loss RF switching and tuning capability to active circuits, which in turn enables tunable amplifiers, filters, and phase shifters.

Sandia's RF microresonators use the lateral active modes in an AlN active layer to achieve high quality factor and low motional impedance for high frequency resonators. Additionally, the use of lateral modes allows the device properties to be defined by photolithography, rather than by film thickness, enabling the fabrication of resonators covering different frequency ranges on a single die. This capability will allow the addition of miniature high-Q filter banks and oscillators to SOI CMOS circuits. Device Q's >1000 have been demonstrated at frequencies up to 1 GHz [6].

These microresonators are fabricated on an SOI substrate, with the oxide layer serving as an etch stop for the release etch of the 2-μm-thick sacrificial silicon layer. The oxide layer provides a well-defined etch-stop to achieve a consistent gap, enabling other devices such as pirani gauges and resonant accelerometers [7] to be fabricated in the same process. The first process step is the deposition of a temperature compensating oxide layer [5], followed by the patterning of tungsten and aluminum lower electrodes. Next, the AlN active layer is deposited by sputtering, followed by the upper Al electrode. Openings are etched in the AlN layer, and selective isotropic dry etching is used to remove the silicon from below the SiO_2 layer of the device film stack.

B. High-Voltage Devices

Sandia has exploited the presence of a buried insulator to fabricate high-voltage devices which could not be realized in bulk silicon. To accommodate challenging form factor requirements, Sandia builds a photovoltaic (PV) technology on SOI wafers. The PV cell is a single junction device fabricated in the device silicon layer. For these devices cells are connected in series to achieve a desired voltage and current output. The device silicon is typically 5-10 μm thick and the BOX is 1-3 μm thick. The PV collection area is built using standard CMOS processing. After forming the PV collection area, a die singulation etch is done through the front-side top dielectric, the device silicon, and the BOX, landing on handle silicon. Subsequent to the die singulation etch, the wafer is patterned on the backside and Bosch etched through 90% of the handle silicon thickness. After the initial Bosch etch, the wafer is submounted with PV side down to another wafer. After submounting, the Bosch etch is completed by landing on the BOX. To enhance collection efficiency, the exposed BOX is metallized so that light incident to the PV cell front side is reflected back through the collection area. The backside metal stack composition and thickness can be tuned to cancel the total stack stress so the finished PV cell is flat upon release from the submount wafer. Using this technology we have fabricated PV cells up to 7.5 mm in diameter and less than 10 μm thick. [8]

C. Optical Devices

Sandia has created ultra-low loss silicon rib waveguides using lightly doped silicon from 250-nm to 500-nm thick on BOX layers of 1μm to 3μm thickness in several waveguide processes. The high crystalline quality of the surface silicon is essential in achieving the low optical losses. In these structure (Figure 1) the surface silicon is the waveguide core material and the BOX provides the lower cladding layer. The upper silicon dioxide cladding is either applied by CVD or grown through oxidation of the waveguide. We have demonstrated ultra low loss silicon rib waveguides in the SOI technology with propagation losses as low 0.02 dB/cm and internal Quality factors (Q) as high as 1.4×10^7. Similar silicon structures can be implanted and annealed to create ultra-low power silicon modulators and switches based on reverse-biased p-n junction fabricated in the high-crystalline-quality surface silicon layer for modulators with record low

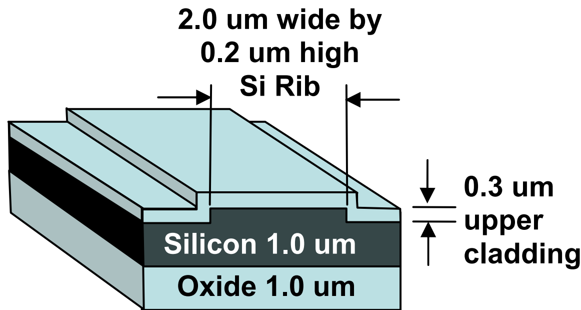

Figure 1. Ultra-low-loss SOI-based silicon rib waveguide exploiting BOX to form the on-chip waveguide.

energies/bit (85fJ) [9]. This technology has also been applied to ultra-compact low-voltage CMOS-compatible high speed microdisk/ring WDM bandpass switches [10] for on- and off-chip optical interconnects capable of providing many Tb/s of bandwidth.

These low-loss waveguides form the basis for optical microring-resonator-based thermal detectors. The detectors are based on the thermo-optic effect and are thermally isolated from a silicon wafer substrate so as to maximize the temperature excursion for a given amount of incident radiation and minimize the impact of thermal phonon noise. The combination of high-Q, thermal isolation, and lack of Johnson noise offers thermal microphotonic detectors the potential to achieve significantly greater room temperature sensitivity than standard bolometric techniques. [11]

D. Atomic/Ion Trapping Quantum Devices

Sandia's microfabricated ion traps represent a conceptual advance for performance standards for hand-held sensors due to the inherent selectivity, sensitivity, and universal applicability of mass spectroscopy as an analytical method. Breakthroughs in simplicity and reductions in the size of mass spectrometers are needed for high-consequence fieldable applications, including error-free detection of chemical/biological warfare agents, medical diagnoses, and explosives/contraband discovery. The array of micro-ion traps is a freely suspended air gap structure fabricated in tungsten using silicon-based semiconductor and MEMS microfabrication methods. In this process, a backside etch that stops on the buried oxide is used to remove the silicon substrate to enable precise, front-side alignment of the through-hole to the ion trap electrode features. These microfabricated ion traps have enabled the capture and manipulation of seven Mg^+ ions for experiments on quantum information processing [12]

E. Contract Stress Sensor

Sandia also fabricates a contact stress sensor on SOI wafers in partnership with Lawrence Livermore National Laboratories. The device functions as a strain gauge in a Wheatstone bridge configuration [13]. A typical starting wafer has 15 µm device silicon thickness and 0.2 µm BOX thickness. The device silicon is patterned, implanted, and annealed to define four discrete resistors that extend into the diaphragm. Controlling the orientation of the resistors relative to the crystal lattice negates lattice effects on the deflection of the diaphragm. After defining the resistors, the diaphragm is defined by pattering and Bosch etching the handle silicon from the wafer backside. The Bosch etch reliably stops on the thin BOX so that the thickness of the diaphragm is defined by the thickness of the device silicon. The diaphragm of the finished device deflects under load and the resulting strain induces a change in resistance. The Wheatstone bridge configuration facilitates an accurate inference of the resistance of the bridge, and that resistance can be calibrated to a known load.

F. Lift Off Devices

It is possible to completely release devices created in the SOI silicon device layer. Sandia has fabricated silicon solar cells with this technique and measured performance equal to standard solar cells. New methods must be developed to assemble these thin (20-µm thick) cells into useful devices and micro-fluidic self-assembly is a potential technique. The advantage of this approach is that the SOI handle wafer can be recycled by growing or depositing a new buried oxide layer and then growing or attaching a new device layer. In this way, the cost of raw materials is dramatically reduced because a whole silicon wafer is not consumed each time.

We have demonstrated a new approach to creating arbitrarily thin crystalline silicon PV cells using standard fabrication techniques combined with MEMS release techniques. The cells are created using standard diffusion steps followed by a deep etch to define the thickness of the cells. The release layer for the cells is a buried oxide sacrificial layer created with an SOI implant approach (e.g. Smart Cut or SIMOX) followed by epitaxial growth of silicon (we are currently collaborating with the National Renewable Energy Lab to develop low-cost epitaxial silicon growth). This method allows reuse of the crystalline silicon material resulting in significant material cost savings. We have demonstrated functional PV cells using this method. These cells have backside contacts to eliminate shading of the cells. (In standard thickness cells, backside contacts provide a 10-15% performance improvement.) The primary benefit of these cells is the reduction in silicon usage. Most of the solar spectrum is absorbed in the first 10-20 um of silicon, the remaining 180 um of material used in standard crystalline silicon cells is primarily for mechanical stability during handling. Further, the kerf loss of this method is at most a few micrometers of silicon per cell layer as compared with the ~150 µm of loss with standard wiresaw and polish techniques. The lift-off technique produces greater than a factor of ten savings in the single largest cost category of solar modules and allows the creation of modules with $\ll$ 1g Si/W_p [14].

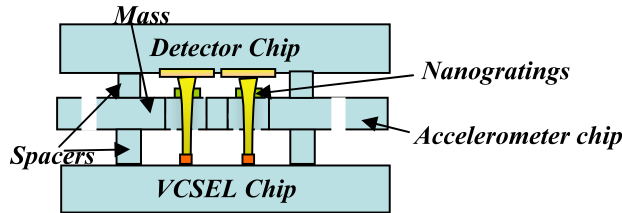

Figure 2. Nano-g Accelerometer Concept

Integration of a variety of technologies has enabled Sandia to develop a new class of highly sensitive, low-noise, low-frequency, ultra miniature (~1mm3) accelerometers based on a nanophotonic sensing mechanism (~10 nano-G/√Hz),. The device concept is illustrated in Fig. 2 In this optical sensing method, sub-wavelength grating structures are coupled in the near-field where very small changes in lateral displacement (femtometers) are detectable as changes in optical reflectance. In this process we integrated large masses built by SOI liftoff techniques to build in-plane accelerometers using these integrated nanophotonic sensors. Gratings were fabricated in a polysilicon surface micromachined process. Inertial sensing proof masses of significant size can be created in SOI wafers. The proof masses of typical MEMS accelerometers and gyroscopes are created by bulk micromachining to achieve the necessary thickness and mass. Sandia has created proof masses of tens of milligrams from SOI wafers by deep reactive ion etching (DRIE) through the 20-micrometer device layer. The release etch removes the BOX, freeing the proof mass. Surface micromachining is used to create sub-wavelength optical gratings which transduce small changes in lateral displacement (femtometers) as detectable changes in optical reflectance. Using this configuration, Sandia has created MEMS accelerometers with record sensitivity (~10 nano-G/√Hz), low noise, and low frequency. Such accelerometers can sense nano-g accelerations, the order of magnitude of the tidal force of the moon on the earth.

III. SUMMARY

Familiarity with silicon-on-insulator (SOI) material over the last two decades led Sandia to explore SOI for more than just high-frequency and radiation-resistant integrated circuits. By exploiting the unique processing capabilities of what is now Sandia's MESA fabrication facility, Sandia has developed a variety of technologies that exploit other chemical and structural properties of SOI to enable alternative technologies for additional functionality beyond those provided by classical integrated circuits.

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