Low Power Silicon Microphotonic Communications for Embedded Systems

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Introduction

Communications links in embedded systems have considerable bandwidth requirements, tight power constraints, and must often remain impervious to electromagnetic interference. Silicon microphotonic communications utilizing wavelength division multiplexing (WDM) and closely integrated with CMOS electronics offers a clear path for addressing many of the performance requirements of these high-performance systems.

Here, we discuss recent results on ultra-low power silicon microphotonic communications with particular emphasis on wavelength division multiplexed (WMD) implementations. In particular we address several key issues associated with implementing WDM communication systems on a chip, and, in particular, issues associated with their application to embedded systems.

A Microphotonic Communication System

To achieve ultra-low power high-bandwidth communications on or between a microprocessor and a high-performance sensor chip, a silicon microphotonic WDM communication system can be closely integrated with the microprocessor or sensor chip. For a complete link, communications between both a high-performance microprocessor and a sensor chip is required. Since it is often necessary to achieve close integration with silicon micro-photonic communications and each of these chips, typically fabricated in dissimilar processes, hybrid integration is preferable to direct integration. Such an approach is depicted in Fig. 1.

Close electrical communications serves two purposes: (1) Short through-silicon-vias (TSVs) provide low capacitance connections to the electronics chip thereby greatly reducing the electrical communications power consumption, and (2) the substantial density of TSVs that can be achieved enables very high data rate electrical communications out to the WDM optical network for longer distance communications.

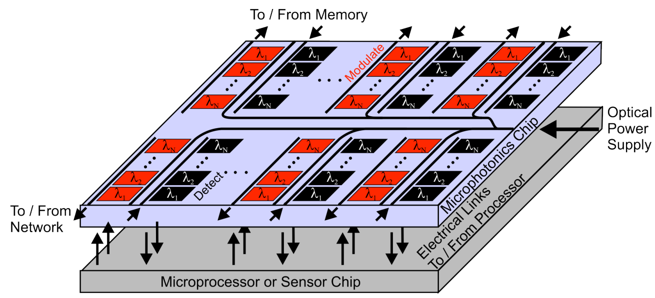

Figure 1: A close, wavelength division multiplexed (WDM) connection between a microprocessor or sensor chip and a silicon microphotonics chip can enable ultra-low power optical communications with unparalleled bandwidth.

Both high-speed silicon modulators [1-3] and germanium detectors [4-6] have been implemented on CMOS compatible platforms and even with direct CMOS integration. However, the emphasis on ultra-low power data communications has only recently emerged as a critical issue in high performance digital systems. As such, many of the initial silicon photonic components were not optimized for very low power digital communications. The power consumption for a silicon microphotonic communication link consists of: (1) power consumption of the modulator and the associated thermal control the WDM system, and (2) the power consumption of the light source and receiver electronics.

At the modulator, we expect to consume ~20fJ/bit for the modulator drive and another 50fJ/bit for the thermal control of the modulator and the associated WDM system. In support of this analysis, we recently demonstrated a new class of silicon resonant modulators that utilize a vertical *p-n* junction with very tight confinement of the optical mode and strong overlap with the depletion region of the *p-n* junction. As a result of the tight confinement and strong modal overlap, we were able to demonstrate a silicon modulator energy-per-bit of only 85fJ [4] with finite-element designs indicating potential for achieving ~20fJ/bit operation. Further, we achieve 10Gb/s depletion-mode operation with a low, 3.5V drive, no signal pre-emphasis, and a bit-error-rate (BER) below 10^{-12}. Finally, the power required to thermally control these modulators and the WDM system can be minimized by directly integrating heaters [7].

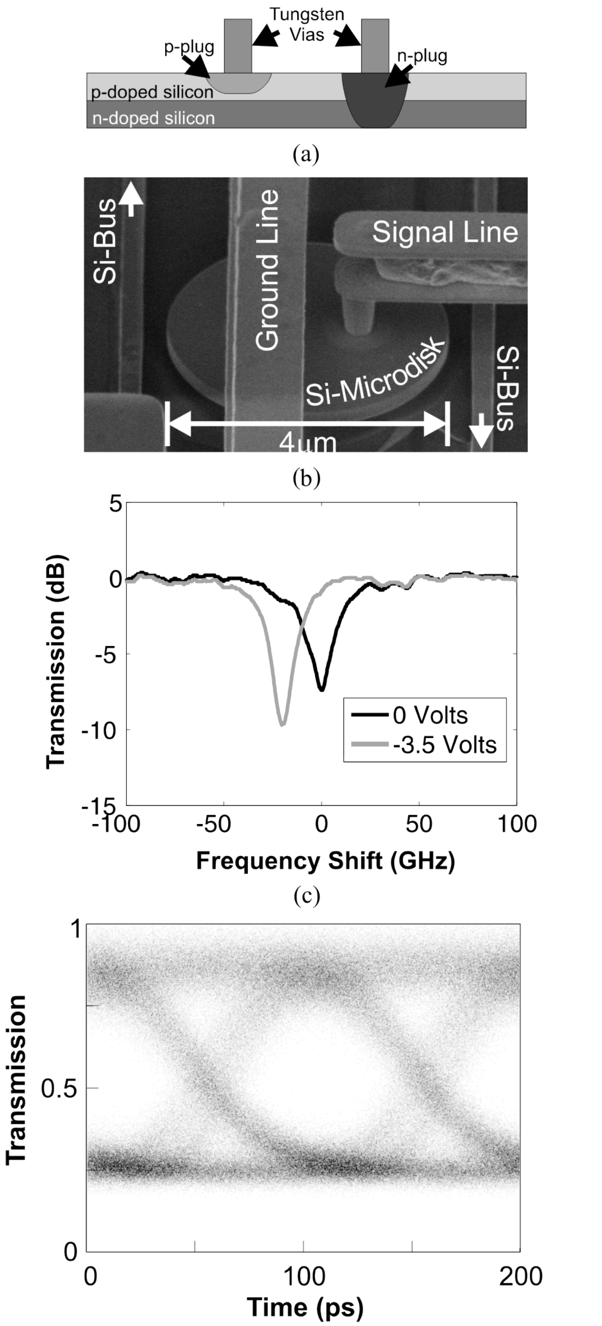

Figure 1. (a) Cross-sectional diagram of the microdisk modulator, (b) a scanning electron micrograph of the fabricated 4μm diameter microdisk modulator, (c) the optical spectra of the microdisk with no bias and a 3.5V reverse bias applied, and (d) an eye-diagram for the modulator with a 10Gb/s NRZ data format with a PRBS pattern length of 2^{31}-1.

From a shot noise based bit-error-rate (BER) analysis, we find that a relatively small number of photons, less than one-thousand (or ~0.15fJ at λ = 1.55μm), are required per bit at the receiver. The main challenge is not fundamental, but rather technological, as achieving very low-capacitance receivers substantially impacts the degree to which amplification is required to achieve 1-Volt signaling. To first order, assuming 10-dB optical loss and a 10% electrical-to-optical conversion efficiency, we expect to require ~30fJ/bit power between the electrical power required to drive the source and the power required for amplification at the receiver.

Conclusions

The need for high data rate, low-power communications in embedded systems is clear. Many significant challenges in the development of ultra-low power WDM silicon microphotonic communications have been surmounted in recent years and we project that upto 1-Tb/s silicon microphotonic communication lines will be demonstrated in the near future an energy consumption of only 100fJ/bit.

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