Silicon photonics manufacturing

William A. Zortman,[1,2,*] Douglas C. Trotter,[1] and Michael R. Watts[3]

[1]*Applied Photonic Microsystems, Sandia National Laboratories, Albuquerque, New Mexico 87185, USA*
[2]*Center for High Technology Materials, University of New Mexico, Albuquerque, New Mexico 87106, USA*
[3]*Research Laboratory of Electronics, Massachusetts Institute of Technology, Cambridge, Massachusetts 02139, USA*
**wzortm@sandia.gov*

Abstract: Most demonstrations in silicon photonics are done with single devices that are targeted for use in future systems. One of the costs of operating multiple devices concurrently on a chip in a system application is the power needed to properly space resonant device frequencies on a system's frequency grid. We asses this power requirement by quantifying the source and impact of process induced resonant frequency variation for microdisk resonators across individual die, entire wafers and wafer lots for separate process runs. Additionally we introduce a new technique, utilizing the Transverse Electric (TE) and Transverse Magnetic (TM) modes in microdisks, to extract thickness and width variations across wafers and dice. Through our analysis we find that a standard six inch Silicon on Insulator (SOI) 0.35μm process controls microdisk resonant frequencies for the TE fundamental resonances to within 1THz across a wafer and 105GHz within a single die. Based on demonstrated thermal tuner technology, a stable manufacturing process exhibiting this level of variation can limit the resonance trimming power per resonant device to 231μW. Taken in conjunction with the power to compensate for thermal environmental variations, the expected power requirement to compensate for fabrication-induced non-uniformities is 17% of that total. This leads to the prediction that thermal tuning efficiency is likely to have the most dominant impact on the overall power budget of silicon photonics resonator technology.

OCIS codes: (130.3120) Integrated optics devices; (220.4610) Optical fabrication; (160.6000) Semiconductor materials.

References and links

1. D. A. B. Miller, "Device Requirements for Optical Interconnects to Silicon Chips," Proc. IEEE **97**(7), 1166–1185 (2009).
2. P. M. Kogge, ed., *"ExaScale Computing Study: Technology Challenges in Achieving Exascale Systems,"* Univ. of Notre Dame, CSE Dept. Tech. Report TR-2008–13, Sept. 28, 2008.
3. Q. Xu, B. Schmidt, S. Pradhan, and M. Lipson, "Micrometre-scale silicon electro-optic modulator," Nature **435**(7040), 325–327 (2005).
4. P. Dong, S. Liao, D. Feng, H. Liang, D. Zheng, R. Shafiiha, C.-C. Kung, W. Qian, G. Li, X. Zheng, A. V. Krishnamoorthy, and M. Asghari, "Low Vpp, ultralow-energy, compact, high-speed silicon electro-optic modulator," Opt. Express **17**(25), 22484–22490 (2009).
5. W. A. Zortman, M. R. Watts, D. C. Trotter, R. W. Young, and A. L. Lentine, "Low-Power High-Speed Silicon Microdisk Modulators," (CLEO) CThJ4 San Jose, Ca (2010).
6. M. R. Watts, D. C. Trotter, and R. W. Young, "Maximally Confined High-Speed Second-Order Silicon Microdisk Switches," in *Optical Fiber Communication Conference and Exposition and The National Fiber Optic Engineers Conference*, OSA Technical Digest (CD) (Optical Society of America, 2008), paper PDP14.
7. B. G. Lee, A. Biberman, J. Chan, and K. Bergman, "High-Performance Modulators and Switches for Silicon Photonic Networks-on-Chip," IEEE J. Sel. Top. Quantum Electron. **16**(1), 6–22 (2010).
8. A. Biberman, H. L. R. Lira, K. Padmaraju, N. Ophir, M. Lipson, K. Bergman, "Broadband CMOS-Compatible Silicon Photonic Electro-Optic Switch," CLEO CPDA11 (2010).
9. A. Barkai, Y. Chetrit, O. Cohen, R. Cohen, N. Elek, E. Ginsburg, S. Litski, A. Michaeli, O. Raday, D. Rubin, G. Sarid, N. Izhaky, M. Morse, O. Dosunmu, A. Liu, L. Liao, H. Rong, Y. H. Kuo, S. Xu, D. Alduino, J. Tseng, H.

#135422 - $15.00 USD Received 21 Sep 2010; accepted 19 Oct 2010; published 26 Oct 2010

F. Liu, and M. Paniccia, "Integrated Silicon Photonics for Optical Networks," J. Opt. Netw. **6**(1 Issue 1), 25–47 (2007).
10. M. R. Watts, W. A. Zortman, D. C. Trotter, G. N. Nielson, D. L. Luck, R. W. Young, "Adiabatic Resonant Microrings (ARMs) with Directly Integrated Thermal Microphotonics," CLEO CPDB10 (2009).
11. C. T. DeRose, M. R. Watts, D. C. Trotter, D. L. Luck, G. N. Nielson, and R. W. Young, "Silicon Microring Modulator with Integrated Heater and Temperature Sensor for Thermal Control," in *Conference on Lasers and Electro-Optics*, OSA Technical Digest (CD) (Optical Society of America, 2010), paper CThJ3.
12. P. Dong, S. Liao, D. Feng, H. Liang, R. Shafiiha, N. Feng, G. Li, X. Zheng, A. V. Krishnamoorthy, and M. Asghari, "Tunable High Speed Silicon Microring Modulator," in *Conference on Lasers and Electro-Optics*, OSA Technical Digest (CD) (Optical Society of America, 2010), paper CThJ5.
13. W. A. Zortman, M. R. Watts, and D. C. Trotter, "Determination of Wafer and Process Induced Resonant Frequency Variation in Silicon Microdisk-Resonators," in *Integrated Photonics and Nanophotonics Research and Applications*, OSA Technical Digest (CD) (Optical Society of America, 2009), paper IMC5.
14. M. R. Watts, D. C. Trotter, R. W. Young, and A. L. Lentine, "Ultralow power silicon microdisk modulators and switches," Proceedings of IEEE conference on Group IV Photonics (Institute of Electrical and Electronics Engineers, New York, 2008), pp. 4–6, 2008.
15. M. Popović, "Complex-frequency leaky mode computations using PML boundary layers for dielectric resonant structures," Integrated Photonics Research, Washington, DC, (2003)
16. R. E. Walpole, and R. H. Meyers, *Probability and Statistics for Engineers and Scientists*, (Macmillan, New York, 1989)
17. Soitec products page: http://www.soitec.com/en/products/soi-products.php
18. International Technology Roadmap for Semiconductors 2009: http://www.itrs.net/Links/2009ITRS/Home2009.htm
19. D. K. Sparacin, C.-Y. Hong, L. C. Kimerling, J. Michel, J. P. Lock, and K. K. Gleason, "Trimming of microring resonators by photooxidation of a plasma-polymerized organosilane cladding material," Opt. Lett. **30**(17), 2251–2253 (2005).
20. J. E. Cunningham, I. Shubin, X. Zheng, T. Pinguet, A. Mekis, Y. Luo, H. Thacker, G. Li, J. Yao, K. Raj, and A. V. Krishnamoorthy, "Highly-efficient thermally-tuned resonant optical filters," Opt. Express **18**(18), 19055–19063 (2010).
21. Y. Zhu, T. E. Müller, and J. A. Lercher, "Single Step Preparation of Novel Hydrophobic Composite Films for Low-*k* Applications," Adv. Funct. Mater. **18**(21), 3427–3433 (2008).
22. S.-M. Lee, D. Cahill, and T. Allen, "Thermal conductivity of sputtered oxide film," Phys. Rev. B **52**(1), 253–257 (1995).

1. Introduction

Future high-density chip-to-chip and high performance computing (HPC) interconnect communications power consumption and off chip bandwidth requirements will be extremely challenging or impossible to meet using electrical interconnects [1,2]. In [1] an energy/bit target of 97fJ/bit (970μW at 10Gbps) is given for the off chip transmitter in a 22nm node chip which is expected to be available in 2015. Recent demonstrations of silicon photonic technology have shown that wavelength division multiplexed (WDM), low energy, high bandwidth interconnect schemes are compatible with existing silicon high volume manufacturing (HVM) techniques in microelectronics even if high volume integration is still in its nascent stage [3–5]. Technologies have begun to emerge that embark on the next step in integrating these discrete devices into systems [6–9].

With large scale integration, devices will be repeated across wafers, lots, and process runs to build systems. The uniformity of these devices is critical since high yield is essential to continue the historic achievement of low cost in silicon parts during the age of optical interconnects. The demonstration of ultra-low switching energies of 3.2 fJ/bit [5] (40μW at 12.5Gbps) in a resonant disk modulator used a single fixed source with optical frequency tuned to the modulator. While important in making modulation power insignificant, systems require many devices that are instead tuned to fixed laser frequencies. This integration costs power to orderly initialize and maintain each resonance on a grid of channels. To impose this order we expect integrated resistive heaters to be used in compensating for manufacturing variation (the subject of this work) which will be referred to as trimming; heating is also needed to compensate for environmental effects which we refer to as tuning. In order to maintain low switching energies for frequencies on an International Telecommunication Union (ITU) grid, for example, manufacturing processes that can match resonator frequencies

#135422 - $15.00 USD Received 21 Sep 2010; accepted 19 Oct 2010; published 26 Oct 2010

to designed targets will enable lower energy off-chip transmit and receive capability for exascale computing and data centers by reducing the integrated heater currents required to actively trim the resonant frequency [10–12]. A low cost system involves not only freedom from special cause variations, but also tight control of process variations so that the modulators, switches (if present), and receiver chips can be matched in WDM systems with their incumbent sources. (Special causes in an otherwise controlled process are single or serial events resulting from failed quality control and are by definition outside the normal process variations. Examples include human error, defects, software failure and tool failure although some of these are catastrophic and may also result in product loss.)

In this work we evaluate the wafer-to-wafer (WTW), within wafer (WIW) and within die (WID) resonant frequency variation on Sandia National Labs' radiation hardened six inch Silicon on Insulator (SOI) 0.35μm process using 248nm lithography. Then we use a new technique to extract the contributors to the variation and use this information along with careful assumptions about future interconnect architecture and current HVM capabilities to make estimates of the total power consumption, including resonant frequency trimming and tuning, for future chip to chip silicon photonic links.

2. Resonant frequency variation across wafers

We previously reported on the process induced WIW frequency variation in [13]. In the current work the within die WID variation is also measured. Additionally, we now present results comparing metalized and non-metalized wafers from two fabrication facility (fab) runs so that we can begin to see if metallization has an impact on resonant frequency variation (e.g. due to strain, evanescent coupling, etc.).

Each wafer in this study had five nominally identical microdisk resonators fabricated on adjacent waveguides with a 75μm separation between each waveguide for a total of five devices across 300μm. The wafers used in this study are labeled W1 and W2; W1 is metalized and contains fully contacted and doped resonators while W2 is silicon only (does not have contacts or doped regions) and both have 5000Å of deposited oxide above the silicon waveguides. This breadth of data gives us the ability to collect statistics on the WID variation and begin to understand the impact of processing beyond the initial etch to the silicon lattice (sometimes called the silicon cut). Additionally, data from [13] is included as W0, which is from a different process run.

The resonator is a 6 micron diameter microdisk with a waveguide to disk separation of 320nm fabricated on 240nm SOI over 3μm buried oxide using the same process as described in [14]. We chose to use microdisks because their resonant frequencies depend only on thickness and diameter, enabling dimensional variations to be easily extracted from the results; furthermore the large free spectral range offered by these small disks separates the resonances sufficiently to avoid confusion when determining the resonant shift between devices. Resonators on all three wafers were measured along the vertical axis of the wafer from the top down to the wafer flat (sometimes called the notch). W1 and W2 had eight die with five identical disks on each die (a total of 40 data points on each wafer). A schematic of the location of each measurement on the wafer is shown in Fig. 1(a). W0 had 12 die along the vertical axis and only one device per die (a total of 12 data points).

#135422 - $15.00 USD Received 21 Sep 2010; accepted 19 Oct 2010; published 26 Oct 2010

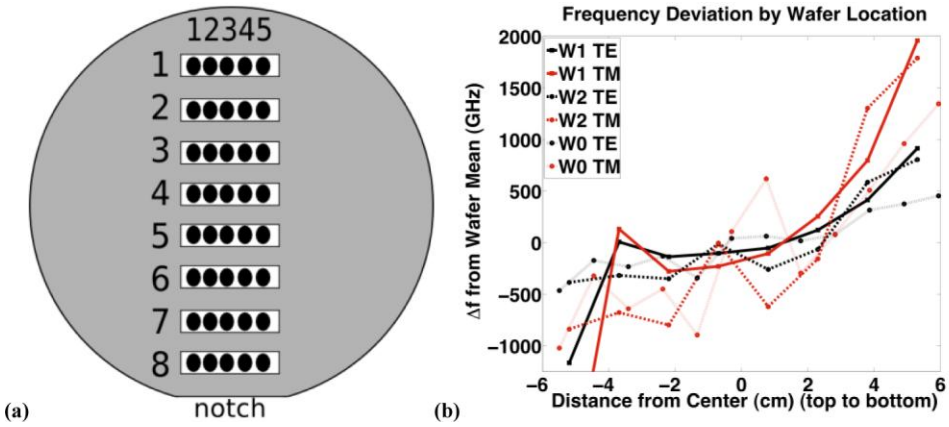

Fig. 1. (a) The layout of the devices that were measured from Wafer 1 and Wafer 2. Wafer 0 only had one device per chip, but followed the same measurement scheme from top to notch. (b) The frequency deviation from the wafer mean by distance from wafer center. All three wafers showed frequency increasing from top to notch and W1 had a statistical outlier chip at the top of the wafer.

Each device was measured using an Agilent 8164B swept laser source with 125MHz (1pm) frequency resolution. Light was coupled on chip using lensed fibers with an on/off chip insertion loss of ~20dB. The chips were temperature controlled at 27°C to within 0.01°C. Measured resonant frequency variation for 30 measurements on the same disk had a three standard deviation (3σ) value of +/–250MHz, which is taken as the resolution of our measurement.

In this paper we only consider variations from the mean and not the variation from the designed resonant frequency because it is assumed that a designer using a well characterized, albeit variable process, will skew mask designs to compensate. Figure 1(b) shows a plot of the TE and TM resonant frequencies from top to bottom along the vertical line of all three wafers. Each W1 and W2 data point is the mean of the five resonators in that die. The TE frequency range is seen to be about 1THz and the TM varies by nearly 2.5THz. We are most interested in the TE modes because the modulators were designed for that polarization, however the TM resonance will be important for Section 3 when the dimensional deviations are extracted. Both wafers show that WIW variation is significant when matching chips within a single wafer. The wider TM frequency range will be discussed in detail in Section 3. Additionally, the trend from lower frequencies to higher across all wafers will be shown in Section 3 to be the result of thickness variation, likely driven by non-uniform planarization that is inherent in the SOI manufacturing process.

Table 1 is a summary of the wafer level data collected for the three wafers and it shows significant WTW and WIW variation that cannot be attributed to metallization. Comparison between wafers shows that there can be >1 THz of variation WTW. W0, which was metalized has a lower standard deviation than W2 (silicon only) and additionally W2 and W0 are closer in mean frequency than W0 and W1, the two metal wafers. The outlier chip from the top of W2 was filtered out of the data and the result of this filtering is shown in parentheses in Table 1. With this point removed the standard deviation falls below the silicon only wafer. The summary in Table 1 shows that while there is significant WTW variation, conclusions about metallization cannot be drawn from a single un-metalized wafer.

When examining the variation WIW and WTW it is instructive to keep in mind the volumes at which chips are manufactured. In microelectronics even an 8 inch HVM memory facility can achieve output levels of 10,000 wafers per week with thousands of dice on each wafer for a total output of millions of dice weekly; this is compounded by the fact that most

#135422 - $15.00 USD Received 21 Sep 2010; accepted 19 Oct 2010; published 26 Oct 2010

manufacturers run several facilities on the same process. It is therefore important to ask if the same level of output will be achieved in silicon photonics because with a large volume of

Table 1. The mean, standard deviation and median for the resonant wavelengths of the devices across the three wafers. Data with the first chip filtered out of W1 is shown in parenthesis

	W0 [metal] From [13]	W1 [metal] (filtered)	W2 [Si only]	|W1-W2|
TE Mean (THz)	192.0	191.0 (191.2)	192.2	1.117
TE Std (GHz)	285	556 (357)	430	126
TE Median (THz)	192.0	191.0 (191.0)	192.0	0.966
TM Mean (THz)	195.8	194.1 (194.5)	194.8	0.666
TM Std (GHz)	741	1,194 (749)	957	237
TM Median (THz)	195.7	194.2 (194.2)	194.4	0.215

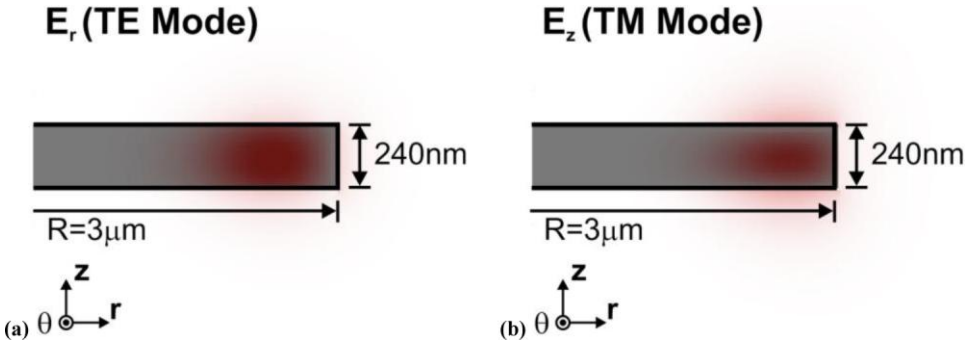

Fig. 2. The (a) TE and (b) TM modal fields (red) used to extract the layer thickness and diameter variations in this study. Both modes exhibit strong confinement in the vertical direction, which results in substantial sensitivity to silicon thickness variations.

Table 2. The predicted frequency deviation is given for a dimensional deviation in both thickness and diameter. Thickness is the dominant driver of frequency variation although diameter is more significant in the pertinent TE modes

Polarization	Thickness	Diameter
TE	–140GHz/nm	–52GHz/nm
TM	–330GHz/nm	–36GHz/nm

dice it should be possible to match chips from different wafers and lots to minimize the chip-to-chip variation; this idea will be explored further below. Therefore, quantifying the WID variation is of interest. To understand the WID variation it is first necessary to quantify what is driving the variation. This is done using a new technique in the next section.

3. Proposal and demonstration of a new technique to extract dimensional variation

In a microdisk, frequency variation is the result of thickness and diameter variations alone. Using a cylindrical modesolver [15] we calculated the modes (Fig. 2) at different diameters and thicknesses to determine their sensitivity to both dimensional variations. In general, the modal frequencies depend on both the mode number and design dimensions and are most accurately represented as a function with the aforementioned dependencies. This function can be expanded in a Taylor series and in cases where the dimensions do not vary substantially from the design dimensions, higher order terms may be dropped. Such is the case in this analysis. The calculated first order sensitivities are presented in Table 2 about a resonant wavelength of $\lambda = 1550$nm.

The sensitivity of both the TE and TM modes to layer thickness variations is much larger than to diameter variations. This is particularly true in the case of the TM mode for which the sensitivity to thickness variations is nearly ten-fold higher than it is to diameter variations. It

#135422 - $15.00 USD Received 21 Sep 2010; accepted 19 Oct 2010; published 26 Oct 2010

is for this reason that the TM modes suffer from much greater frequency variation across each wafer [Fig. 1(b)].

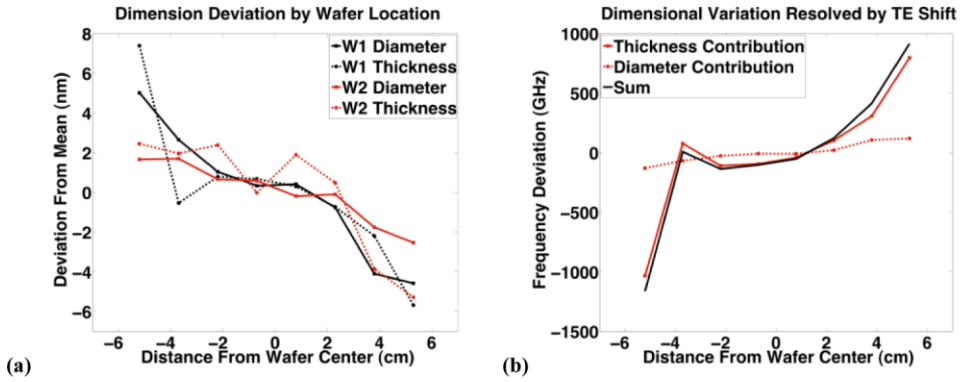

Fig. 3. (a) Thickness and diameter variations from the mean across W1 and W2 after extraction from the frequency data using Eq. (1). (b) The reconstructed TE variation in W1 showing the strong influence that thickness variation has on TE frequency.

To definitively isolate the cause of the resonant frequency variation, we can write the pair of equations describing the TE and TM resonant frequencies in matrix form. Since this matrix represents a linear invertible system of two equations and two unknowns, it provides for a unique solution. The measured frequency variations are on the right side and the mode solver prediction from Table 2 in the 2x2 matrix on the left. The two unknowns, ΔT and ΔD are the disk-to-disk thickness and diameter changes respectively, which are in the vector that completes the system:

$$\begin{bmatrix} \left.\frac{df}{dT}\right|_{TE} & \left.\frac{df}{dD}\right|_{TE} \\ \left.\frac{df}{dT}\right|_{TM} & \left.\frac{df}{dD}\right|_{TM} \end{bmatrix} \times \begin{bmatrix} \Delta T \\ \Delta D \end{bmatrix} = \begin{bmatrix} \Delta f_{TE} \\ \Delta f_{TM} \end{bmatrix} \quad (1)$$

By inserting the data from W1 and W2 from Fig. 1(b) into the right side of Eq. (1) the dimensional variations can be extracted.

The results of the calculation are plotted in Fig. 3(a), which shows the dimensional variations that are driving the frequency variations from Fig. 1(b). W0 was eliminated for clarity. W1 has a larger diameter variation although within 3cm of the center of the wafer the difference is not significant from W2. Figure 3(b) shows the reconstructed TE frequency shift for W1 as the sum of the thickness and diameter variations. Diameter deviations on W1, although larger and contributing 250GHz of variation are less significant when considering the edge thickness contribution which is 2THz as depicted in Fig. 3(b). Eliminating the outlier reduces that variation to 1THz.

4. Within die variation

The data from Section 2 can be averaged for each chip (a total of 8 averages) on W1 and W2. Then each resonator on each die can be compared to the die average to calculate the WID variation using all forty measured data points (5 points per die). This provides forty data points per wafer and through the use of Eq. (1) we can then calculate an average within die variation, which is plotted in Fig. 4(a). Thickness variations within die are limited to +/–0.1nm, which is expected over such a small distance. Resonator diameter variations are unexpectedly severe with close to +/–0.35nm variation on average across a 300μm distance and both wafers follow a similar trend from device to device for diameter variation.

#135422 - $15.00 USD Received 21 Sep 2010; accepted 19 Oct 2010; published 26 Oct 2010

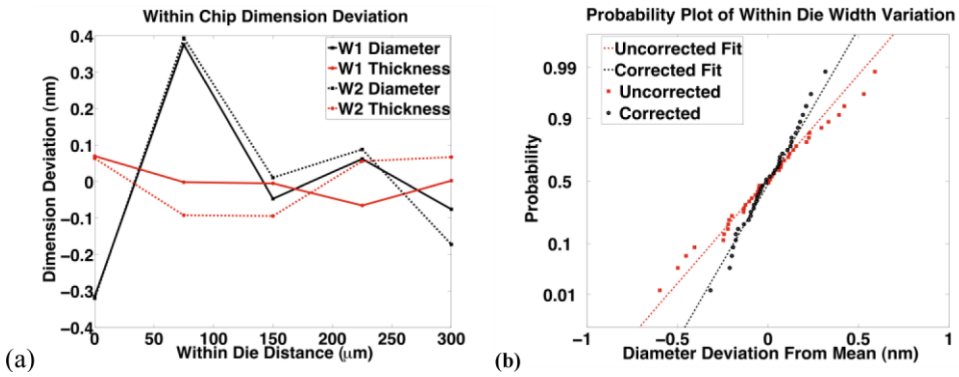

Fig. 4. (a) The average dimensional variation within the dice shows that diameter variations are consistent from wafer to wafer leading to investigation of the mask error special cause. (b). After residual analysis to remove the special cause variation the diameter is controlled to within +/–4Å on a die.

The repeatability of the WID trend on two wafers shown in Fig. 4(a) is hypothesized to be caused by a mask error (a special cause) as consistent printing of the same feature sizes would explain the error repeatability across sixteen dice on two wafers. An analysis of variance (anova) test of the WID variation of the mean for each disk shows that

the diameters for each disk do not come from the same distribution with a probability of this being the case being well below 1% (P-value<0.01) suggesting a special cause is driving the variation as opposed to the normal process variation. (Anova is a statistical tool for comparing more than two distributions using methods similar to the two sample t-test which compares two distributions. Both tests determine if the difference in the mean of the data sets is significant and can be used to determine a probability, or P-Value, that this significance exists. That is, they test if the data in two or more groups come from the same distribution. In this case, the anova is being used to assess the probability that there is an absence of special cause variation.) [16]

When data is driven by a special cause then we may attempt to remove that variation by performing a residual analysis [16]. The residual analysis on this data was done using a polynomial fit of the trend from die to die. The data is then subtracted from the fitted line giving each point a residual value. The normal probability of occurrence for the dimensions are shown in Fig. 4(b); the probability plots show the uncorrected diameter data and corrected diameter data indicating the improvement of the Gaussian nature after residual analysis is performed. It also shows that the distribution for the corrected data is tighter. Analysis of the lithographic mask production showed that the drawn error of the mask computer aided design (CAD) file is +/–0.7nm due to the grid snap error on the printed silicon feature, which is close to the error between the average mismatch from disk 1 to disk 2. Other physical special cause or even process variations arising in mask manufacture may be attributed to the variation in the other three disks because even process errors on the mask would turn into special causes in the fabrication facility. Modern HVM fabs use ebeam cut masks with smaller snap resolution. It is conceivable that this error could be mitigated in such facilities. Therefore, the residual probability plot of diameter corrected data (black dots) in Fig. 4(b) is a good estimate of the achievable WID diameter variation within our manufacturing process.

An anova test and residual analysis were also performed on the thickness data. The anova test shows a confidence value of 0.8, a high confidence that the thickness data comes from the same distribution and not providing justification for using residual analysis. In Fig. 5(a) frequency probability plots of the within die frequency variation reconstituted from corrected dimensional data using Eq. (1) are done for uncorrected data, width corrected data and, for completeness, thickness corrected data as well. Figure 5(b) gives the diameter

#135422 - $15.00 USD Received 21 Sep 2010; accepted 19 Oct 2010; published 26 Oct 2010

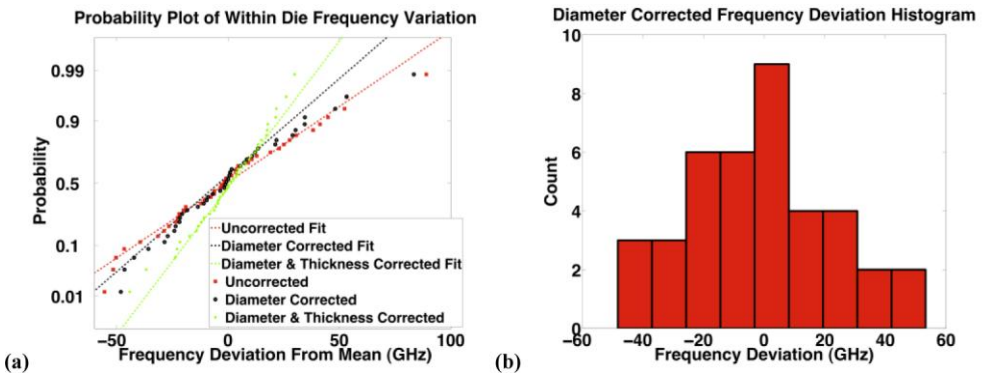

Fig. 5. (a) After residual analysis on the diameter variation, 105GHz frequency variation is found to be the capability of our process. When thickness is also corrected the deviation drops to close to 70GHz, but evidence of a special cause driving the thickness variation was not found. (b) The diameter corrected data in histogram format. Matched silicon photonic chips would still have to tune out the within die frequency deviation and on average tune across a 50GHz range when using a 0.35 micron process.

corrected plot in histogram format. The thickness variation may in fact be caused by a trend as we see in Fig. 3(a) from the top to the bottom of the wafer, but this could not be confirmed across 300μm. Not surprisingly, even though we can improve the diameter contribution by a factor of 1/3 through elimination of special cause variation, it does not improve the within die frequency variation by more than about 10%, as most of the frequency variation is caused by SOI thickness variation.

5. The Impact of non-uniformity

We maintain that the WID variation (as opposed to WIW, WTW or run to run (RTR)) is an accurate metric for understanding the impact this would have on an integrated system of silicon photonic chips. In early dual core microprocessor technology, high volume manufacturing automation systems could match single core chips that had similar speeds for packaging together of a dual core product. Because microelectronic silicon fabrication facilities sort every chip they produce, this automation (with development of an optical probe card) can be used to match transmitter, switch and receiver chips to limit the system variation to the within die variation. Switching chips do present a greater challenge because they have to be matched to more transmit and receive chips. Using only the three wafers we have tested it is possible to match micro-disk resonators of two chips to within 7GHz and 42% of the chips match within 25GHz. In volumes on the scale of server chips, matched parts will still be commodities and tighter matching will be possible.

Given the progress of manufacturing automation technology, specifically the ability to match manufactured chips, we will use the entire distribution (105GHz), minus the one outlier, of width corrected WID variation of the 0.35μm process to make estimations on the impact to the power consumption. Elimination of outliers is acceptable because on a commercial device it is reasonable to expect manufacturers to print duplicate waveguides side by side on a chip and use the one that has the smallest variation. This method of binning is common in flash memory manufacturing. It is unclear at this time if our process can be improved upon, although we expect improvement from ongoing efforts.

Modern HVM will provide improvement to the overall uniformity, although what specific improvements we can expect is unclear because tool and technique advances to make rectangular transistors on sub 100nm thick silicon does not translate into quantifiable gains with circular resonators using 220nm thick silicon. For example SOI manufacturing can achieve +/–3nm thickness variation on 70nm thick 300mm wafers; for 200nm, 70 nm thick wafers have variation of about +/–7nm wafer sizes [17]. This seems to indicate that the

#135422 - $15.00 USD Received 21 Sep 2010; accepted 19 Oct 2010; published 26 Oct 2010

evolution in the silicon equipment industry planarization tools (from the 200mm generation to the 300mm generation) has reduced uniformity effects for thin SOI, but comparative values between 300mm and 200mm for thick SOI are not available. Additionally, this is WIW data, not WID. For diameters, the International Technology Roadmap for Semiconductors consistently specifies a 30% improvement in critical dimension uniformity per node because gate lengths continually scale by a factor of about 30% per node [18]. This is for patterning of rectangular structures with a field length of 33mm. The ability of 193nm immersion lithography, resists, hard-masks and modern etch equipment could not be found for circular structures. To use this data for optical resonators would require assumptions about geometry, thickness and translation of WIW statistics to WID statistics although there is certainly some gain to be realized from the progress in silicon electronics. Therefore, techniques, statistics and specifications germane to silicon photonics, such as those presented here, will be developed on the photonic side and provide conclusive uniformity data for 250nm thick SOI on 300nm wafers processed with tools at the 22nm node or below.

For frequency trimming, heater technology is assumed although other techniques have been proposed [19]. In order for all of the devices based on heated micro disk/ring resonators to be relevant in a thermally varying system such as a CMOS chip in a server environment they will have to be designed so that the resonant frequency is higher than the source when the server is running at the maximum value of the specified temperature range. This will ensure sufficient margin to allow an integrated heater to reduce the resonant frequency to match the source. This would place the laser line at the far left end of Fig. 5(b). So when the server chip environment is at its maximum temperature the resonator at the bottom of the frequency distribution will be several GHz above the laser source and require some amount of power to match the channel. The frequency distribution will then dictate additional heating for the other resonators proportional to the size of that distribution. A wider distribution creates a larger penalty. A distribution penalty figure of merit P_{δ} exists such that:

$$P_{\delta} = \frac{R}{2}\eta_H \tag{2}$$

In this equation, R is the range of the frequency distribution (GHz) and η_H, the heater efficiency (W/GHz). Division by 2 is used because on average we only have to trim across half of the distribution if it is Gaussian. Note that 3σ, or some other measure of the breadth of the data, can replace R, if outlying resonators can be disabled or discarded without corrupting other channels. This term merely represents the breadth of resonator frequencies that must be considered.

The impact of manufacturing non-uniformity to a resonant device can be applied to modulators or passive filters. Modulator switching energy is insignificant because gate level voltage switching at 12.5Gbps using only 40μW has been demonstrated [5]. What is left is trimming for manufacturing variation and tuning because of thermal environmental effects. For both trimming and tuning heater efficiency, η_H, of 4.4uW/GHz is used as demonstrated in [10]. For trimming, assuming 105GHz frequency variation across a chip, the distribution penalty, P_{δ}, is 231μW. For tuning, a server environment is assumed with an average 25°C temperature variation where we use 10GHz/°C of resonant frequency shift. This yields 1.1mW for a grand total including modulation, trimming and tuning of 1.371mW, which means trimming represents 17% of the total power per resonant device. Looking at the energy picture for 12.5Gbps the average power corresponds to 110fJ/bit, which is 12% above the 2015 target given in [1]. At speeds above 14Gbps this goal would be met.

An important outcome from this analysis is that improving heater efficiency is the primary channel for lowering power consumption in these devices. It addresses the largest contributor to power consumption, temperature tuning, and also indirectly, the second largest, trimming to compensate for manufacturing variation. In addition to the tethering technique in [10], effort to improve resonator insulation using backside etch has been demonstrated [20]; silicon

#135422 - $15.00 USD Received 21 Sep 2010; accepted 19 Oct 2010; published 26 Oct 2010

electronics research into porous dielectrics [21] and thermally tailored sputtered oxides [22] provide further promise if optically sound analogs can be found.

6. Summary

In evaluating the power costs of systems built with demonstrated devices in silicon photonics, we evaluated a six inch SOI 0.35μm process to quantify the frequency variation across runs, wafers and dice. The process has 1THz within wafer variation in the TE mode resonance. By comparing the TE and TM resonant frequency variations in microdisk resonators, it has been demonstrated that the primary driver of resonator non-uniformity is SOI thickness variation, as opposed to diameter variations, which can exceed 10nm across a wafer. Through the use of this technique special cause variation was extracted from the within die measurements and eliminated by residual analysis to demonstrate a 105GHz range within a 300μm distance printed on a single die. Although our process can likely be improved upon to reduce lithographic and other deleterious patterning and processing effects, SOI thickness nonuniformity remains the primary driver of resonant frequency nonuniformities in microdisk resonators.

Based on this result the estimated non-uniformity driven power consumption is 231μW which when added to thermal tuning for environmental considerations is 17% of the total power consumed per resonant device. This result applies to both modulators and passive filters. Therefore, the largest impact to reducing power consumption in resonant silicon devices will come from improvements in thermal tuner efficiency.

Acknowledgements

Sandia is a multiprogram laboratory operated by Sandia Corporation, a Lockheed Martin Company, for the United States Department of Energy's National Nuclear Security Administration under contract DE-AC04-94AL85000.

#135422 - $15.00 USD Received 21 Sep 2010; accepted 19 Oct 2010; published 26 Oct 2010