Low-Power High-Speed Silicon Microdisk Modulators

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Abstract: A novel silicon microdisk modulator with "error-free" ~3 femtojoule/bit modulation at 12.5Gbs has been demonstrated. Modulation with a 1 volt swing allows for compatibility with current and future digital logic CMOS electronics.
OCIS codes: (130.3120) Integrated optics devices; (230.5750) Resonators; (230.7370) Waveguides.

1. Introduction

Microdisk resonators have been proposed for high speed and low energy optical interconnect integration with CMOS electronics. Silicon photonic optical modulators with speeds up to 10Gb/s and energy as low as 50fJ/bit have been reported [1,2]. The modulator presented here demonstrates both increased bandwidth and reduced power dissipation by further reducing the physical size, introducing new doping geometry and reducing the applied voltage from a small negative to a small positive voltage that is less than the built-in potential of the device.

2. Analysis

The bandwidth limitation in reverse biased depletion mode modulators is currently driven by the RC time constant. Likewise, the energy consumption of the reverse biased modulator can be decreased through reduced capacitance leading to smaller devices. Speed increases and energy savings can be gained by making the active PN junction region as small as possible through selective doping of the modulator periphery as in Figure 1A. This modulator is a 3.5μm disk contacted near the center as in previous designs [1]. However, in this design, the PN diode is only implanted around the periphery of the device limiting junction capacitance to that area. The charge must be extracted by following this same peripheral line which is a limitation when the PN junction doping goes around the entire 2π radians of the disk. However, by limiting the doping to only π radians of the device, resistance is cut in half allowing for higher speed operation. The Q of the device is also increased by decreasing dopant induced loss. This results in a smaller required shift to get the necessary extinction for error free operation. Even though the index shift, δn/n, is in theory only half as much as if the device was doped over 2π radians, at high-speed larger devices do not fully deplete the charge in such a large area as a result of the increased resistance and capacitance. In effect, a device that is completely peripherally doped cannot take advantage of the index shift around the entire device at high speed and by only doping half of the disk, the free-carrier losses are reduced, enabling higher-Q resonances.

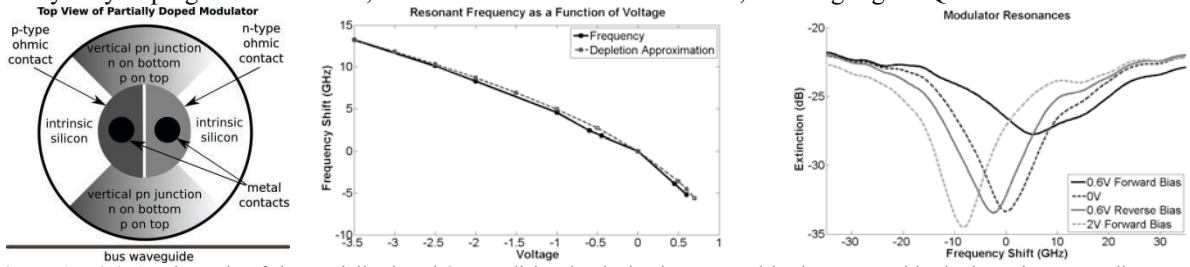

Figure 1 – (A) A schematic of the partially doped 3.5μm disk. The device is contacted in the center with ohmic regions extending out to the active, index shifting portion of the device. This design limits the area where junction capacitance applies. (B) The solid line shows the measured resonant frequency as a function of voltage and, for comparison, the normalized depletion width change for ~10^{18}/cm^3 dopant density as a function of voltage. (C) The resonances for selected points that were plotted in (B).

The method used to drive the device reduces the drive voltage and therefore, the consumed energy-per-bit. Devices driven in forward bias are usually bandwidth limited by the carrier lifetime in the depletion region and pass current 50% of the time in a non return to zero coding scheme. Reverse bias devices are limited by carrier sweep out times from the depletion region, which is a much faster effect. However, larger voltages (2.5V – 3.5V) are required to move enough charge from the neutral region to create a suitable index shift. From the depletion approximation it is known that the depletion region widens as the square root of voltage so each incremental voltage shift in the reverse bias results in less effect. However, by driving the modulator slightly into the forward bias, but below the built in potential, the depletion region is reduced (charge is stored), but little current is passed. In this mode of operation a larger amount of charge is moved with smaller shifts in voltage compared to a reverse biased device, but the speed of response is not limited by the carrier lifetime because sub-turn-on voltage allows the persistence of a

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built in field similar to a reverse biased device. The capacitance of the device is increased over what it would be if the device was operated only in reverse bias, but the carrier concentration change (and thereby index change) is the same in either case for a given shift in the resonance. Because the energy per bit is $E=CV^2/4$, driving down the required voltage more than offsets the slightly increased capacitance enabling a significant reduction in energy-per-bit. Fig. 1B shows this process as it generates the plasma-optic index shift [3] resulting from depletion region widening (charge extraction). The depletion region expansion for 1.2 V shift from 0.6V to -0.6V results in a frequency shift of 9 GHZ as compared to the 2V required to get a similar shift in only reverse bias. Figure 1C shows actual resonances measured with a swept laser source at 0.6V, 0V, -0.6V and -2V.

3. Experimental Results

The device fabrication is the same process flow as described in [1]. Devices were tested using an Agilent 8164B tunable laser source coupled into the chip using Nanonics lensed fibers. The disk is modulated through the use of a 50 ohm terminated probe driven at 12.5Gbs by the Centellax 1B1-A 10G BERT with peak to peak amplitude of 0.9V, 1.2V and 1.4V. No bias is applied. The output signal is amplified using an Amonics L-band amplifier. Bit error rates with 2^{31}-1 PRBS are measured using a high speed photodetector and the Centellax BERT.

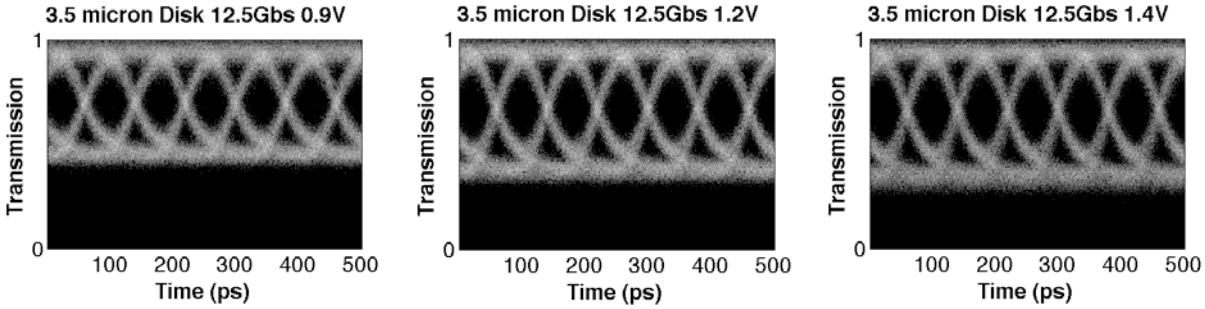

Figure 2 – (A) Unfiltered eye diagram for the partially doped modulator at 0 bias with a peak to peak amplitude of 0.9V on the drive signal. Extinction is 4dB with wide open eye. (B) The same modulator driven at 1.2V peak to peak amplitude and 0V bias this time demonstrating 5dB of extinction. (C) The modulator driven at 1.4V with 6dB of extinction.

The eye diagram in Figure 2A demonstrates the 12.5Gbs performance at the three voltage amplitudes shown. These voltages were chosen because they correspond to the minimum amplitude for 4dB, 5dB and 6dB extinction respectively for increasing voltage. Greater extinction is possible by increasing the voltage, but this would require a bias-T to move the center voltage into reverse bias. Based on our testing, amplitudes beyond 1.5V without any reverse voltage on a bias-T result in enough forward current to slow the charge response. The threshold voltage for this device is about 0.9V, however at 0.75 volts 60uA of current is flowing compared to 30uA at 0.7V. All three drive amplitudes resulted in error free operation at 12.5Gbs with 2^{31}-1 PRBS for 200 seconds which is when testing was halted.

Energy measurements were done with Time Domain Reflectometry (TDR) on a Tektronix DSA. For a drive amplitude of 1V (from 0.5 forward bias to 0.5 reverse bias) the energy measured is 3fJ/bit. The TDR pulse is only available in 0.5V increments and measurements at 0.75 volts are confounded by the presence of a more substantial (60uA) subthreshold current. The results were compared to an analytical model that uses the depletion approximation capacitance for the diode, ohmic regions and fringes [4]. The analytical result of 3.8fJ/bit compares favorably with the measurement.

4. Conclusions

By shrinking the active region in a 3.5um silicon microdisk and introducing a new bias regime 12.5Gbs, 1V, error free operation was achieved resulting in energy performance of ~3 fJ/bit. These low voltage modulators can be driven directly at logic-level from a CMOS chip, greatly simplifying CMOS modulator driver design.

Sandia is a multiprogram laboratory operated by Sandia Corporation, a Lockheed Martin Company, for the United States Department of Energy's National Nuclear Security Administration under contract DE-AC04-94AL85000. This work was funded by DARPA's Microsystems Technology Office (MTO).

5. References

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