Monolithic Integration of Silicon Electronics and Photonics

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Abstract: A low power modulator is monolithically integrated with a radiation hardened CMOS driver. This integrated optoelectronic device demonstrates 1.68mW power consumption at 2Gbps.
OCIS codes: (130.3120) Integrated optics devices; (230.5750) Resonators; (230.7370) Waveguides.

1. Introduction

Since the early demonstrations of silicon micro-ring resonant devices researchers have advanced the advantage these devices would have when integrating with existing silicon electronics [1]. For instance, silicon photonic chips have been proposed as optical backplanes for multi-core or multi-chip systems [2]. One of the advantages of using optics is lower power transmission of data as compared to electronic methods [3,4]. In this demonstration, the low power modulator from [3] has been integrated with a radiation hardened complementary metal oxide semiconductor (RADHARD CMOS) process.

2. Design and Fabrication

The disk design shown in Fig. 1(a) is the same as that described in [3]. The disk is a 4μm diameter resonator with waveguide to bus separation of 320nm. Contact is made in the center with the highly doped ohmic contact regions extended to the edge of the whispering gallery mode region of the device that reduces both resistance and capacitance. The disk operates on the plasma carrier dispersion effect [5] by depleting carriers in a vertical PN junction through reverse bias.

Fabrication was done on Sandia's RADHARD CMOS Microelectronic Development Lab (MDL) using six inch Silicon on Insulator (SOI) wafers and 248nm lithography with 0.35μm minimum feature width. The silicon thickness is 250nm with 3 μm buried oxide. The CMOS process was not changed for this demonstration although a few steps were added to the normal disk manufacturing process. In the fabrication of most CMOS devices a dielectric island is used to protect the active areas during initial transistor isolation processing. A dielectric layer was used to protect the silicon disk and waveguide as well in this case. Additionally, the modulator was doped with separate implants (from the CMOS) and a typical dielectric film was deposited over the optical waveguides to protect them during additional CMOS processing. Previous demonstrations of this disk technology [3,6] have shown more than 14dB resonance depth with high Q of about 10^4. The additional processing steps have reduced the Q to 10^3 and resulted in a resonance that is only about 4dB deep likely due to contributed surface roughness from the additional processing.

The disk was integrated with inverters comprising a ten-stage CMOS driver with the final stage connected to the signal line of the modulator. The inverter chain has a fanout of zero. An L-edit snapshot of the layout can be seen in Figure 1(b). The CMOS operates with a 3.3V supply (V_{dd}) and threshold voltage on the gate of 1.6V (V_t), although the resonator has been demonstrated to operate with 1V of drive strength.

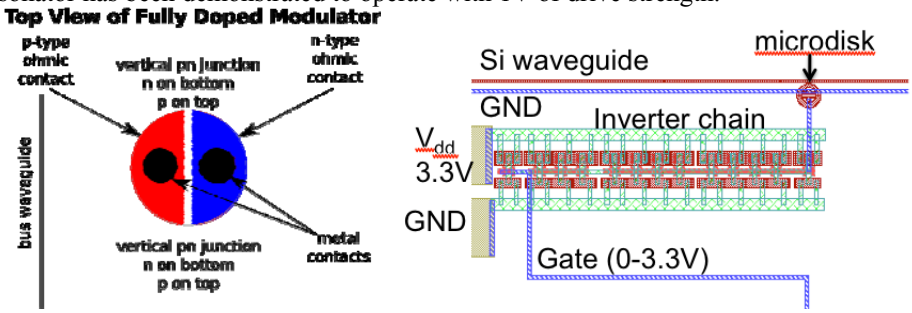

Figure 1 – (a) A schematic of the 4μm disk. The device is contacted in the center with ohmic regions extending out to the active, index shifting portion of the device. This design operates in reverse bias, limits the area where junction capacitance applies and ensures large mode overlap with the depletion region by use of a vertical PN junction. (b) The microdisk is shown in an L-edit snapshot integrated with a 10 stage CMOS inverter chain. The inverter chain has a fanout of zero.

3. Experimental Results

Devices were tested using an Agilent 8164B tunable laser source coupled into the chip using Nanonics lensed fibers. The CMOS gate is driven through contact pads by the use of an un-terminated probe driven with a V_{pp} amplitude of 3.3V. The signal source is the amplified output of a Centellax 1B1-A 10G BERT (bit-error-rate-tester) and a bias T is used to set the waveform level. V_{dd} is connected to a DC source and held at 3.3V. The output signal is amplified using an Amonics C-band amplifier. Bit error rates with 2^{31}-1 PRBS are measured using a high speed photodetector and the BERT.

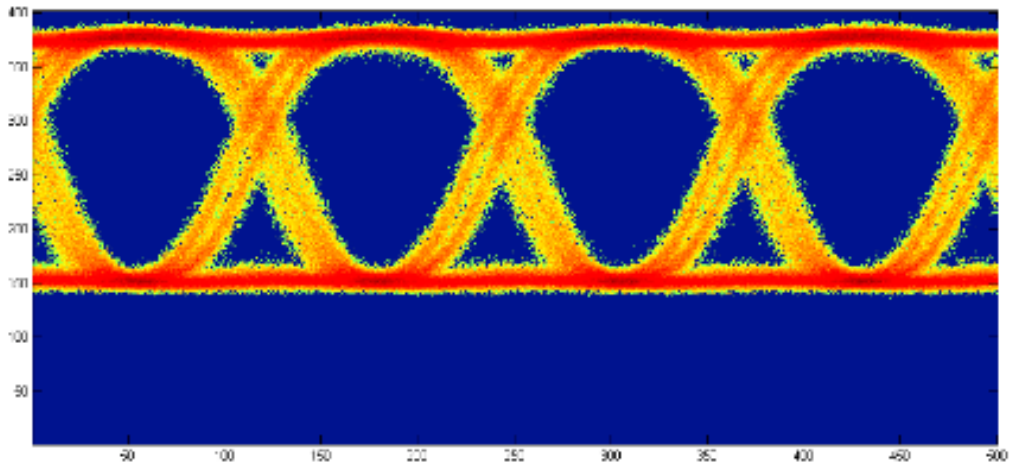

Figure 2 – (A) Unfiltered eye diagram with peak-to-peak amplitude of 3.3V on the drive signal. Extinction is 4dB with wide open eye. The bit error rate is <1e-12. The intersymbol interference is caused by the bandwidth limit of the inverter chain.

The eye diagram in Figure 2A demonstrates the 2Gbps performance of the CMOS, although the modulator has much higher bandwidth. The extinction ratio is almost 4dB. Because the disk has the capability to run at 10Gbps it is possible to realize the full extinction of the resonance when the CMOS inverter switching bandwidth limits the speed. The intersymbol interference may be caused by the inverter bandwidth limitation. Circuit simulation verified this effect showing incomplete depletion of the gate at 2Gbps. The device was run for five minutes error free for a BER of $<10^{-12}$.

At 3.5V the disk resonator consumes ~50fJ/bit as confirmed by time domain reflectometry and analysis. At 2Gbps this is 100μW. The total power consumption measured as the current passing through the DC probe times V_{dd} is 1.68mW (840fJ/bit).

4. Conclusions

Demonstrations of this type exhibit the potential to integrate silicon photonics and electronics in space or other radiation intense environments where high off chip data rates and low power are needed.

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5. References

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