Low-voltage differentially-signaled modulators

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Abstract: For exascale computing applications, viable optical solutions will need to operate using low voltage signaling and with low power consumption. In this work, the first differentially signaled silicon resonator is demonstrated which can provide a 5dB extinction ratio using 3fJ/bit and 500mV signal amplitude at 10Gbps. Modulation with asymmetric voltage amplitudes as low as 150mV with 3dB extinction are demonstrated at 10Gbps as well. Differentially signaled resonators simplify and expand the design space for modulator implementation and require no special drivers.

OCIS codes: (130.3120) Integrated optics devices; (250.6715) Switching; (200.4650) Optical interconnects; (250.7360) Waveguide modulators.

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1. Introduction

Recent demonstrations of ring and disk silicon micro-resonators continue to build the case for these devices as compact, low power and high-speed solutions for chip-to-chip optical interconnects [1–11]. These efforts have demonstrated very low power consumption (and energy-per-bit) as well as single volt drive which makes these devices compatible with current complementary metal oxide semiconductor (CMOS) drive voltages. Even lower drive voltages have been proposed in [11] for devices operating in forward bias although they pull a direct current. The advantage of low drive voltage is that while the International Technology Roadmap for Semiconductors (ITRS) predicts V_{dd} levels to drop to 710mV in 2019, recent work [12,13] has suggested that in order to reduce power in exascale supercomputers to reasonable levels, transistor supply voltages may need to be lower than ITRS predictions. 500mV chip supply rail levels are a possibility and demonstrations have shown logic gates that can be run with V_{dd} as low as 350mV [14]. In order for optics to function with the low drive voltages proposed and the lower power demanded by exascale data centers and high performance computing (HPC) applications, both low voltage and low power are necessary. Both of these are possible in a reverse biased device.

Additionally, future chip designs may have low voltage signaling (LVS) on chip or rely on LVS for off chip signaling. (LVS here refers to the general application of low voltage lines operating using a differential pair which includes many standards such as current mode logic (CML), voltage mode logic (VML) and low voltage differential signaling (LVDS) to name a few. LVDS levels have declined with CMOS supplies for several years in compliance with Joint Electron Devices Engineering Council (JEDEC) guidance.) Differentially signaled lines for memory access have already replaced the traditional front side bus on contemporary processors [15]. Recent research into on chip LVDS technology has demonstrated 5Gbps with <400mV signal amplitude [16,17]. Although the more pertinent figure may be that after attenuation these lines terminate with less than 100mV of amplitude meaning a photonic device taking this signal beyond the chip stack may have to operate with voltages at this level. Signal conditioning in the electronics would not be eliminated and terminating with optics may not always be convenient. LVS on chip is evolving to take a greater role for intra-chip interconnections; optics providing inter-chip interconnections should be able to

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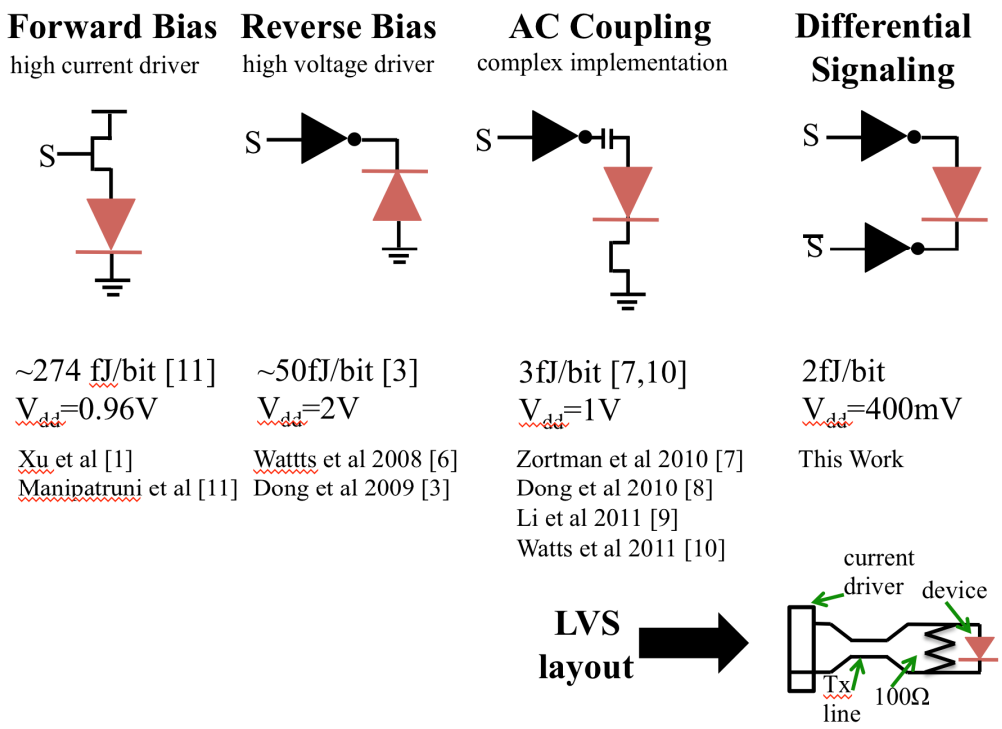

Fig. 1. Circuit schematics of the different signaling regimes proposed for silicon photonic resonant modulators. The first modulators were driven with forward bias and require a high current driver. Next reverse biased devices were introduced that require high voltage drivers to function. AC coupling, taking advantage of both forward and reverse bias operation is very low power, but the circuit implementation is more complex. Either a transistor or diode (or some element) must be placed between the modulator or inverter and ground to maintain the desired bias point. Differential signaling is implemented with inverters and no special drivers. Energies/bit are given for each modulator with selected references to show the effect that signaling has had on this metric. Finally, a possible LVS schematic is shown. Forward bias, reverse bias and AC coupled designs do not have straightforward LVS implementations. Differential signaling is inherently LVS compatible.

operate at these low voltages. Affording the capability for direct differential signaling of a photonic device widens the design space available for their implementation.

We recently demonstrated a micro-disk modulator that is compatible with LVS and operates in reverse bias [7,10]. Here, we use this low power modulator design in conjunction with differential signaling. We show, that symmetrically driven, the devices can operate at 3fJ/bit [7,10], 10Gbps and 500mV amplitude with 5dB extinction, or 400mV with 4dB extinction with a wide range of common mode voltages on the differential inputs. With asymmetric drive it is possible to drive the devices with 150mV to realize an extinction ratio of 3dB and energy consumption of <1 fJ/bit at 10 Gbps. Sub femto-joule operation has not been demonstrated to our knowledge for a modulator of any type. For each demonstration the bit error rate (BER) is $<10^{-12}$ using a 2^{31}-1 psuedorandom bit sequence (PRBS). It should be emphasized that this demonstration is of a new signaling scheme that does not result in any energy reduction, because the voltage on device remains the same. Extinction ratio and speed are not improved as that attribute is best addressed by optimizing Q and dopant distributions [9]. Importantly, this demonstration increases the design space for implementation in future reduced V_{dd} server chips and continues on the improvements we have made to signal these devices over the years and we turn to that forthwith.

Figure 1 gives an overview of select previous work on signaling in silicon photonics and the potential application of this new differential signaling technique's compatibility with

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typical CMOS layout and also LVS technology. Power, or energy/bit, and voltage have both received due attention. Yet the improvements in power, while helped by design evolution, have mostly been the result of the reduced voltages for signaling and these are almost exclusively the result of improved signaling schemes, which we describe and compare in Fig. 1. Here we also consider these improvements in the context of the circuits required to implement each scheme showing that differential signaling is the preferred method, not just for low voltage application, but also for ease of integration into existing signaling regimes. Examining Fig. 1 it is evident that all of the regimes, except AC coupling, have relatively straightforward implementation in CMOS. AC coupling suffers from the need to integrate a capacitor and to maintain a constant voltage offset from ground using a circuit element to compensate for the inverter transfer function current swing. Further, AC coupled transmitters require encoding so that they don't go to an undefined state during idle. Forward bias and reverse bias circuits are easily implemented, but high voltage or high current drivers are required increasing the DC or AC power of the transmitter. Differential signaling is implemented with a complementary circuit that adds power consumption equal to a second inverter and signal line, but the lower driving voltage on each offsets this. Furthermore, on-chip implementations of LVS, should they exist, can be directly terminated into these devices as is. This eliminates receiver circuit implementation and allows easy conversion of LVS transmitted data to the optical domain for longer distance transmission. In light of the fact that LVS signals may attenuate, we show operation well below ITRS predictions is possible with the acknowledgment that any implementation of LVS circuits is not simplified by termination in a photonic device, but that it is the easiest integration of the signaling schemes to do this so far demonstrated in silicon photonic resonant modulators. In summary, two implementations are possible, LVDS termination and two differentially driven inverters operating at predicted V_{dd} levels.

2. Device design and electrical connection

The tested device can be seen in Fig. 2 with the associated contact pads below the drawing of the device. The cross section and manufacturing process are very similar to [6,7,10]. It is a 3.5μm diameter disk built in 250nm thick silicon on 3 μm of buried oxide and then over-clad with 5 μm of deposited oxide. The ohmic contact regions are doped to $10^{20}/cm^3$ and electrically contacted using tantalum lined tungsten contacts. The diode region is built over π radians of the device using a single mask layer with N and P dopants implanted using different energies creating a vertical depletion region. By limiting the dopants to just π radians the current path is shorter and higher modulation speed can be obtained. The bus waveguide is 400nm wide and its mode is horizontally coupled to the disk across a 350nm gap.

The device is driven using two signals that are 180° out of phase as shown in Fig. 3(a). The signals can be referred to as *S* and *S-bar*. *S* refers to the 0 phase signal being driven and it is connected to the anode (P-type). *S-bar* refers to the inversion of that signal, or the signal *S* 180° out of phase, and it is connected to the cathode (N-type). In a differential driving scheme the voltage on each line can be cut in half using *S* and *S-bar* signals with matched phase creating two times the differential swing on each line in the pair. Diagrams of the signals used can be found in Sections 3 and 4, Figs. 4–8. The device is probed using a GSGSG dual signal probe that has 50Ω termination on each active line to ground. A picture of the pad layout and metal lines is given in Fig. 2. The probe contacts Al pads with 30fF of capacitance to ground. Minimum distance (~100μm) aluminum interconnects are used to connect the pads to the optical modulator diode which can be represented as 1600Ω of resistance in line with 15fF. The capacitance has been measured with an HP 4284A using a de-embedding circuit and this agrees with the simulated and analyzed values.

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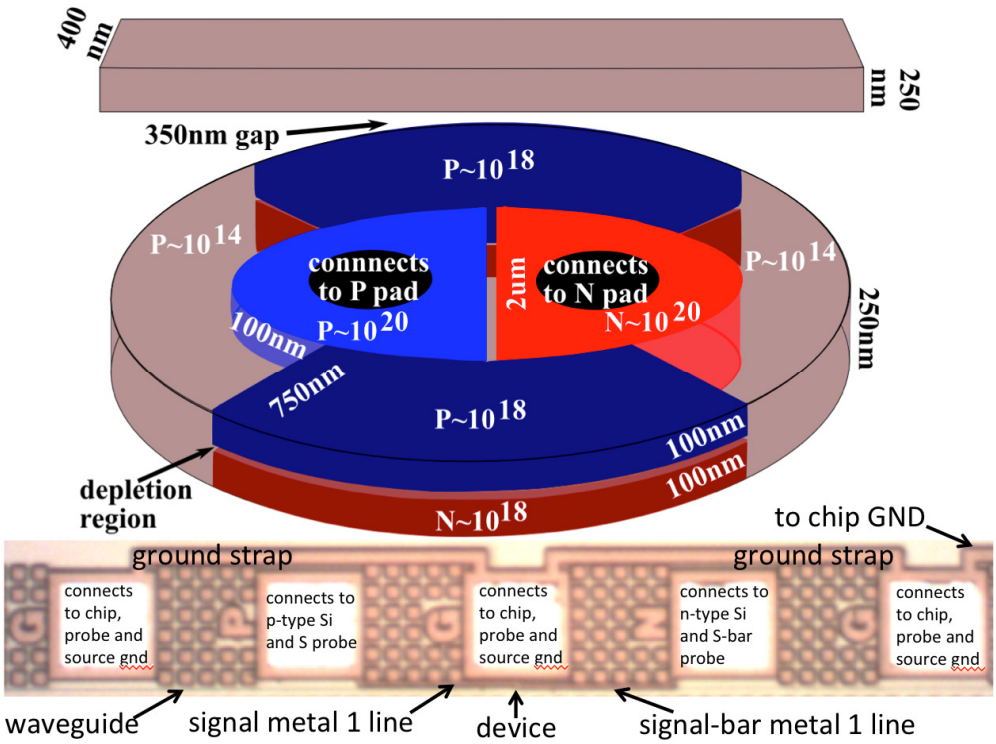
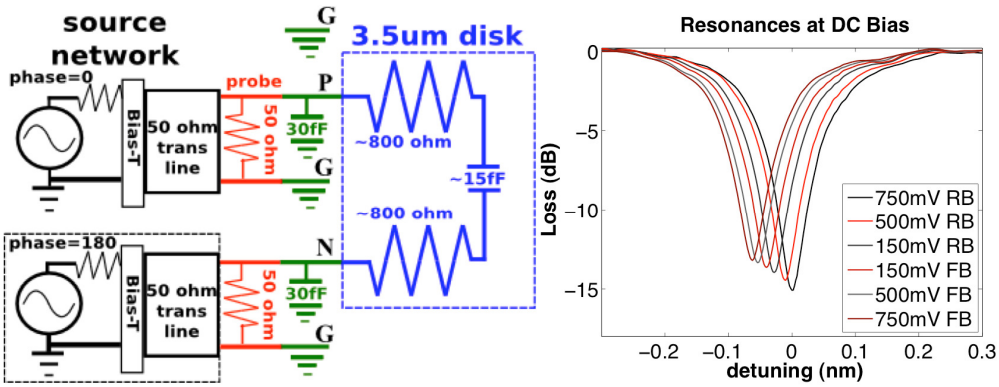


Fig. 2. 3.5 micron diameter disk resonator with photograph of the pad layout. Fabrication is done using 250nm thick silicon on 3µm oxide. There is an overclad of 5µm deposited oxide. The P-type ohmic contact is ~100nm thick and the N-type is the full thickness of the silicon and both ohmic regions are 2µm wide. The depletion region is vertical. The 10^{18} diode doping covers π radians. There is a 350nm gap between the bus and disk. The pad layout shows ground pads all connected to chip and probe ground, yet not connected to the modulator. The P and N pads are signal pads, S and S-bar, and they connect to the modulator as labeled in the disk drawing.



(a) (b)

Fig. 3. Schematic of the pad layout and DC resonances **(a)** The equivalent circuit diagram shows identical drivers 180° out of phase connected through two 50Ω transmission lines to a probe terminated with 50Ω. The pads have a capacitance of 30fF and the modulator is a 15fF capacitor in series with 1600Ω of resistance. Ground pads run to chip ground and the P and N pads are connected as photographed and drawn in Fig. 1. **(b)** The DC resonances of the modulator show a Q ~10^4. For modulation the laser line is put at the 3dB point on the red side of the modulator.

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There is no additional aluminum interconnect required for this device. Each signal pad has a capacitance to ground with half the voltage of a single ended device and in an implementation could be flip-chipped using very low capacitance pads. The additional ground lines that are present ease probing, but do not add to the capacitance present in the interconnect; they are not contacted to the device. They run to the chip ground and their presence is not necessary in implementation on CMOS. This inherent strength of differential signaling means that the microprocessor ground could be different from a stacked photonic chip ground and that ground bounce impact is minimized.

3. Symmetric drive

For both symmetric and asymmetric drive conditions, light from an Agilent 8164B tunable laser was coupled into the photonic chip using lensed fibers. Referring to Fig. 3(a) electrical drive was from the differential outputs of a Centellax TG1B1-A bit error rate tester (BERT), through a bias-T on each line and this signal was driven into the device using Cascade Microtech 50Ω terminated Infinity GSGSG probes. The optical output from the laser was 6dBm with ~10dB coupling loss both onto and off of the silicon die, resulting in a signal level of −15dBm at the output of the chip when the laser source is off resonance. The devices were measured with an insertion loss of 3dB (as is standard in these types of measurements) on the red side of the resonance. Optical power is −18dB emanating from the output waveguide off chip in the '1' state. During modulation this is reduced to 21.1dBm when the extinction ratio measured on the scope is 5dB and this output power scales by approximately ½ dB with 1dB changes in extinction ratio. Inspection of Fig. 3(b) shows that these values are to be expected with the insertion loss dictated at 3dB. The modulated output optical signal was amplified back to 0dBm using an Amonics Erbium Doped Fiber Amplifier (EDFA) for eye analysis in a Tektronix DSA8200. The BER testing was done after conversion back to the electrical domain in an external Nortel PP-10G 11Gbps detector. The Tektronix scope has an internal detector. The eye diagrams and bit error rate measurements are unfiltered in the electrical and optical domain. The eye diagrams are open and all data was recorded using a 2^{31}-1 pseudo-random bit sequence (PRBS) yielding a bit error rate of $<10^{-12}$ in every case. This PRBS test is typically associated with 10Gbps protocols such as Synchronous Optical Networking (SONET) OC-192.

In Fig. 2(b) we show DC symmetric electrical coupling of the device using an arbitrary common mode voltage for both signals. The input voltage for each plot in 2b-2g oscillates around this common mode, which can be arbitrarily chosen. The eye diagrams in Fig. 6(b)–6(d) are for input common modes of 0V, 1.25V and 1.5V which is consistent with AC coupling, VML and CML respectively although the latter two use larger amplitudes in industrial applications. Note that whatever common voltage is chosen, the device always sees a voltage across the contacts of 500mV, either in forward bias (one state – logic 1) or reverse bias (the other state – logic 0), corresponding to a voltage change across the device of 1 volt. The different common modes were obtained by using the bias-T to shift each line equally. The nearly indistinguishable eye diagrams verify that the device is capable of receiving differential signals with a multitude of common modes, rendering the same results and affording compatibility with different standards or simply taking complementary signals from two inverters. In the 500mV amplitude symmetric tests 5dB extinction is obtained when measured from the middle of the top rail to the middle of the bottom rail. This result differs from the extinction in [9] because the insertion loss is greater by choice and the data rate is slower here. Differential signaling is a method to allow optical modulation with reduced voltage on signal lines and can therefore function with the low V_{dd} values predicted by ITRS, but will not increase extinction ratio for a given voltage applied to the device.

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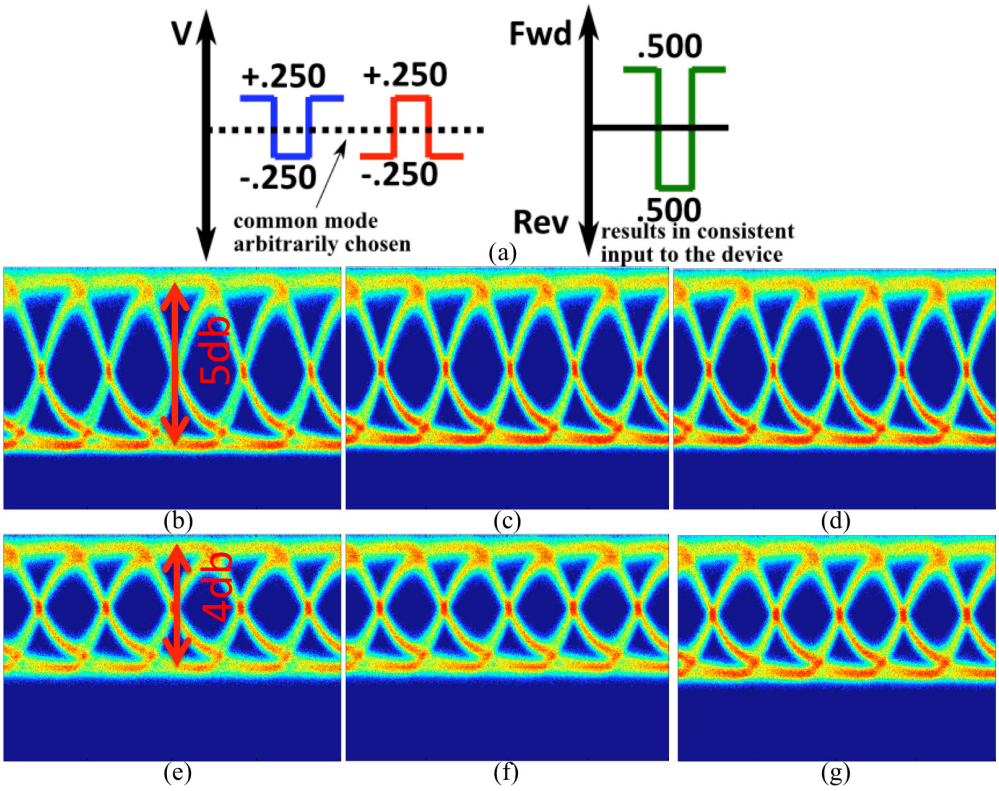

Fig. 4. DC coupling of the device at three common modes. **(a)** The common mode of the drive (dotted line) is varied from 250mV to 800mV to 1.2V always resulting in the same differential signal on the device. Eye diagrams for common modes of **(b)** 0mV, **(c)** 1.25V and **(d)** 1.5V at 500mV show the same 5dB extinction verifying the flexibility of the device to DC couple at arbitrary voltage levels. For 400mV the same common modes are shown in (e), (f) and (g) for an extinction of 4dB. The voltage levels and amplitudes in these last three figures show compatibility with both CML and VML signaling.

To obtain compatibility with LVDS we also demonstrate the performance with a 400mV swing on each line for a total of 800mV into the device in Figs. 2(e), 2(f) and 2(g). The common mode voltages are the same. In the figures it is clear that the extinction degrades with lower voltage, however 4dB is still achievable when measured from rail to rail. The bandwidth limitation of the device introduces a power penalty for each of these examples that we calculate to be 2dB in the 500mV case and 2.5dB in the 400mV case.

Importantly, even though the measurements were performed with a bias tee (that is each side is AC coupled), the differential driving technique described here allows for DC-coupled operation with simple standard differential drivers of a variety of designs (LVDS, LV-CMOS, VML, CML). Additional testing at common mode voltages below 1V, compatible with current and future V_{dd} levels, also yielded eye diagrams that were indistinguishable from those seen in the figures.

4. Asymmetric drive

Figures 5–8 show the driving scheme and the resulting eye diagram for drive amplitudes of 750mV down to 150mV using an asymmetric drive. This approach is not readily transferable to commonly used differential signaling standards nor does it lend itself to simple circuit implementation. However, we found that we could drive the modulators with 150mV signals using this technique although with 500mV signals the performance is comparable to the symmetric case. The concept is to drive a modulator more into forward bias than reverse bias

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with small enough amplitude so as not to go beyond diode turn on and still maintain a small built in field across the depletion region that allows carriers to be swept out without recombination, which occurs in further forward bias and would limit the electrical bandwidth. In this way, small voltages take advantage of the square root function of depletion width which changes most efficiently just below diode turn on [10,17]. As in the symmetric case, differential signaling is used, but the lines have asymmetric common modes. The resulting device bias is the voltage on the anode (blue) minus the voltage on the cathode (red). So for the first figure, two differential 750mV signals still result in a 1.5V differential signal on the device although the actual voltage levels are shifted as shown in green. By applying positive voltage to the cathode (red) and a mix of positive and negative signals on the anode (blue), the signal is pushed into partial reverse bias as shown in green in Fig. 3. This method of biasing the cathode is used in each of the four demonstrations. As the voltage amplitude drops below 300mV it is possible to drive the modulator only in forward bias, yet below the diode turn on. Note that although the 300mV signal can achieve a 4dB extinction as with the 400mV symmetric case, it is noisier. We believe that the noise is the result of more free carriers being present in the sub-threshold forward bias domain. The extinction ratios are 6dB for the 750mV signal, 5dB for 500mV, 4dB for 300mV and 3dB for 150mV.

In the asymmetric case there is also a bandwidth limitation in addition to the introduction of the aforementioned noise. From these two factors the associated penalty is calculated to be 2.9dB in the 750mV case, 2.4dB in the 500mV case, 3dB in the 300mV case and 6.3dB in the 150mV.

The plots show the performance that is available if free level shifting of drivers can be obtained. For example, to obtain the results in Fig. 5 it would be necessary to create a –200mV bias on the output drive of the transmitter chip. This may be desirable, however it requires drivers without a common mode voltage. The enhanced noise in forward bias could be reduced with mask filtering or band-pass filtering.

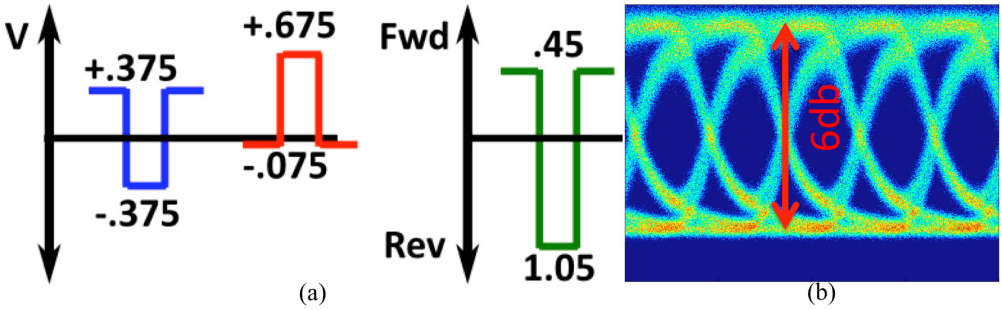

Fig. 5. **(a)** 750mV drive amplitude on both the P (blue) and N (red) silicon contacts on device. The resulting 1.5V amplitude signal is shown in green to be slightly reversed biased because of the 300mV negative bias driven into the N silicon through the use of a bias-T. **(b)** The corresponding 10Gbps eye diagram shows 6dB extinction.

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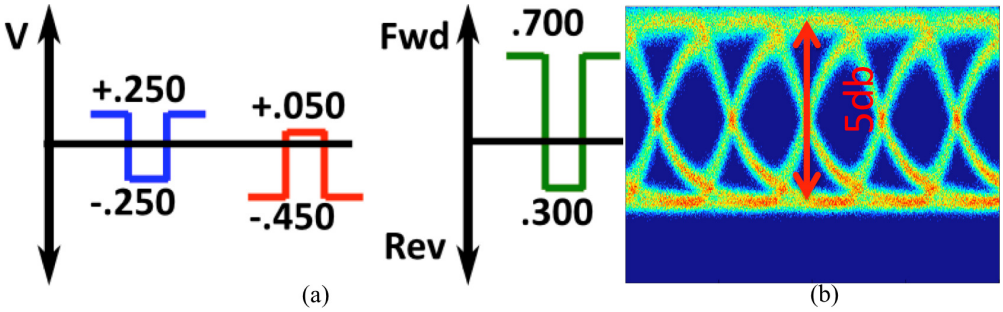

Fig. 6. **(a)** 500mV drive amplitude on both the P (blue) and N (red) silicon contacts on device. The resulting 1V amplitude signal is shown in green to be slightly forward biased because of the 300mV positive bias driven into the N silicon through the use of a bias-T. The slight forward bias is beneficial because the depletion region expands according to the square root of the voltage applied. **(b)** The corresponding 10Gbps eye diagram shows 5dB extinction.

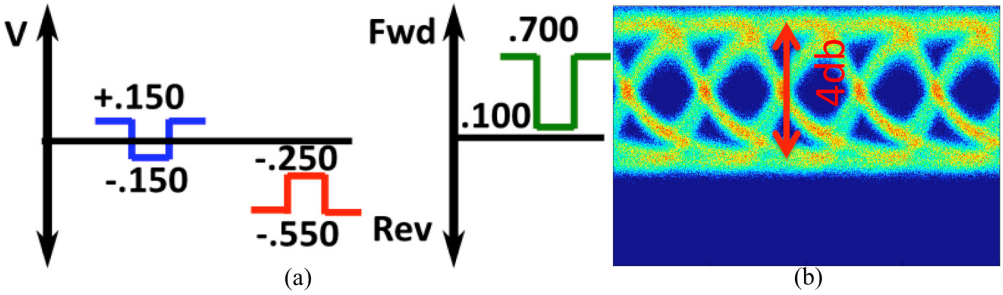

Fig. 7. **(a)** 300mV drive amplitude on both the P (blue) and N (red) silicon contacts on device. The resulting 600mV amplitude signal is shown in green to be only forward biased because of the 400mV bias driven into the N silicon through the use of a bias-T. The forward bias is beneficial in the diode sub-threshold region because the carrier extraction is driven by depletion region expansion instead of carrier lifetime enabling the **(b)** 10Gbps eye diagram shown on the right with 4dB extinction.

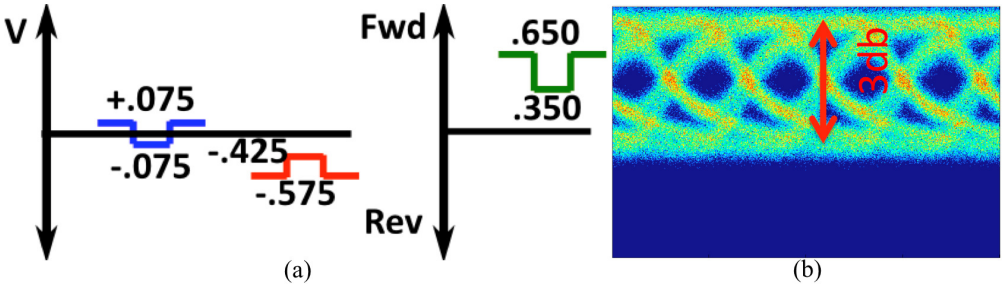

Fig. 8. **(a)** 150mV drive amplitude on both the P (blue) and N (red) silicon contacts on device. The resulting 300mV amplitude signal is shown in green to be only forward biased because of the 500mV bias driven into the N silicon through the use of a bias-T. The forward bias is beneficial in the diode sub-threshold region because the carrier extraction is driven by depletion region expansion instead of carrier lifetime enabling the **(b)** 10Gbps eye diagram shown on the right with 3dB extinction.

5. Energy-per-bit

The energy-per-bit is calculated using the full amplitude of the voltage on device. The energy-per-bit has been measured using time domain reflectometry (TDR) in ½ volt increments. TDR is a decades old technique and its application to the measurement of switching energy is fully described in [10]. Additionally an analytical estimation of capacitance was obtained using the depletion approximation [9,17], which was supported by integrating the simulated charge

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movement in DAVINCI software from Synopsys [10]. In particular, energy results are based on integrating the voltage over time in the case of TDR measurement, calculating the energy from $E = CV^2$ in the analysis, and integrating the charge over time in the simulations. In each case, the energy-per-bit is equal to the measured energy divided by 4, because the probability of switching from 0 to 1 is only ¼ of the total switching space (00 **01** 10 11) in a Non-Return-to-Zero (NRZ), Pseudo-Random Bit Stream (PRBS). Finding good agreement among the different methods here and in [10] we report the energy per bit values in the symmetric case to be 3fJ/bit for 1V swing (500mV drive amplitude) and 2fJ/bit for the 800mV swing (400mV drive amplitude signal). These energies are for the device itself plus a W plug set as interconnect caps are subtracted using de-embedding circuits. The energy does not include the amount that would be required for tuning in a thermally varying environment or the laser power. TDR is executed by integrating the reflection of a finite pulse so there may be additional energy consumed in strings of 1's longer than 2.5 bit slots and that is not captured, but this is no more than 1% of the amount given here.

In the case of the asymmetric drive the energies are approximately the same for the 500mV drive amplitude. For the other cases we find 8.8 fJ/bit for 1.5V swing (750mV drive signal), 1.2fJ/bit for 600mV swing (300mV drive signal) and 900aJ/bit (0.9 fJ/bit) for the 300mV swing (150mV drive signal). The TDR measurements are executed in 500mV increments. Therefore the 800mV, 600mV and 300mV results are scaled for the voltage. We chose to use TDR measurements in this case that begin with a higher forward bias component and then scale the voltage backwards resulting in overestimates of energy consumption, but this is a minor error.

6. Summary

Differential signaling in silicon photonic resonant modulators provides a promising method of realizing both the low voltage CMOS and low current and low voltage drivers envisioned for enabling exascale computing. The symmetric drive capabilities demonstrated here are compatible with typical low voltage differential signaling techniques in that they have been tested with the same common mode voltages and voltage swings as common techniques such as LVDS, CML and VML. Implementation of low-voltage differentially-singaled modulators greatly eases implementation, eliminates special drivers and expands the design space enabling simple implementations such as differential inverter sets. Additionally, asymmetric coupling of the modulators is shown to be a potential path to lower modulation voltages. Symmetrically driven, the modulator uses as low as 2fJ/bit with differential drive signal amplitudes of 400mV. Asymmetrically driven, 900aJ/bit can be obtained with 150mV of drive signal amplitude. In both cases, the silicon modulators operate at 10Gbps with BER $<10^{-12}$ and 2^{31}-1 PRBS patterns.

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