Silicon Modulator with Low Voltage Differential Signaling

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***Abstract*— For exascale computing, optical interconnects will need to operate using low voltage and low power. Here, a differentially signaled silicon resonant modulator is demonstrated with 7dB extinction using 3.2fJ/bit and 500mV signal amplitude at 10Gbps.**

Keywords - silicon photonics, modulator, interconnect

I. Introduction

Recent demonstrations of ring and disk silicon micro-resonators continue to build the case for these devices as compact, low power and high-speed solutions for chip to chip interconnect [1-5]. However, to date, the devices have been driven either (1) at low voltages in forward bias, requiring pre-emphasis for operation at 10 Gbps and above [1,5], (2) in reverse bias requiring voltages significantly above the standard CMOS logic levels [2], or (3) in reverse bias but with a forward voltage achieving low voltage and energy, but requiring AC coupling to achieve both positive and negative voltage across the device [3,4]. We present a demonstration of the latter modulator [3] driven with low voltage differential signaling, enabling low energy consumption and compatibility with both existing and future CMOS drive levels. Importantly, a low voltage differential driver can be designed in standard CMOS logic without the need for complex pre-emphasis circuits, high voltage drivers (with inferior transistors), or large and potentially un-realizable AC coupling. An additional consideration is that while the International Technology Roadmap for Semiconductors (ITRS) does not predict V_{dd} below 700mV until 2024, recent work [6] has suggested that to reduce power in exascale supercomputers, transistor supply voltages may need to be lower than ITRS predictions. Thus, 500mV chip supply rail levels are possible and logic gates with V_{dd} as low as 350mV have been demonstrated [7]. Our demonstration is compatible with those levels.

II. Device Design

The tested device can be seen in Figure 1 and is described in the caption. The cross section and manufacturing process are very similar to [2]. The device is driven using two signals that are 180° out of phase. The signals can be referred to as *S* and *S-bar*. *S* refers to the 0 phase signal being driven and it is connected to the anode (P-type). *S-bar* refers to the inversion of that signal, or the signal *S* 180° out of phase, and it is connected to the cathode (N-type). In a differential driving scheme the voltage on each line can be cut in half using *S* and *S-bar* signals with matched phase creating two times the differential swing on each line in the pair. A diagram of the signal used can be found in Figure 2 of the next section. The device is probed using a GSGSG dual signal probe that has 50Ω termination on each active line to ground with one signal connected to the p-contact of the diode and the other to the n-contact. The probe contacts Aluminum pads with 30fF of capacitance to ground. Aluminum interconnect is used to connect the pads to the optical modulator diode which can be represented as 1600Ω of resistance in line with ~25fF.

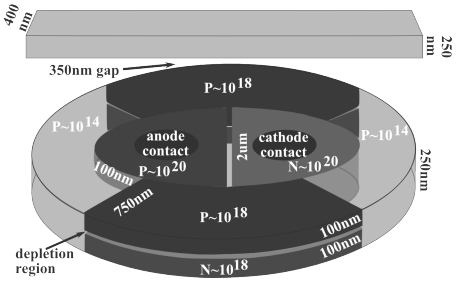

Figure 1 The disk is fabricated using 250nm thick silicon on 3µm buried oxide. There is 5µm deposited oxide over the device and waveguide. The P-type ohmic contact is approximately 100nm thick and the N-type is the full thickness of the silicon. Both ohmic contact regions are 2µm wide at the maximum and doped $10^{20}/cm^3$. The depletion region is vertical and the $10^{18}/cm^3$ diode doping covers π radians of the device. There is a 350nm gap between the silicon bus and waveguide.

III. Experimental Setup and Results

Light from an Agilent 8164B tunable laser was coupled into the photonic chip using lensed fibers. The electrical drive was from the differential outputs of a Centellax TG1B1-A bit error rate tester (BERT), through a bias-T on each line and this signal was coupled into the device using Cascade Microtech 50Ω terminated Infinity GSGSG probes. The optical output from the laser was 6dBm with 10dB coupling loss both onto and off of the silicon die. The modulated output optical signal was amplified back to 0dBm using an Amonics Erbium Doped Fiber Amplifier (EDFA) for eye analysis in a Tektronix DSA8200. The BER testing was done after conversion back to the electrical domain in an external Nortel PP-10G 11 GHz detector. The Tektronix scope has an internal detector. The eye diagrams and bit error rate measurements are unfiltered in the electrical and optical domain. The eye diagrams are wide open and all data was recorded using a 2^{31}-1 pseudo-random bit sequence (PRBS) yielding a bit error rate of $<10^{-12}$ in every case. This PRBS test is typically associated with 10Gbps protocols such as Synchronous Optical Networking (SONET) OC-192.

In Figure 2 we show DC symmetric electrical coupling of the device using an arbitrary common mode voltage for both signals. The input voltage for each plot in

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Figure 2 oscillates around this common mode, which can be arbitrarily chosen. The eye diagrams in Figure 3 are for input common modes of 0V, 1.25mV and 1.5V, which is consistent with AC coupling, VML and CML respectively although the latter two use larger amplitudes. Note that whatever common voltage is chosen, the device always sees a voltage across the device of 500mV, either in forward bias (one state – logic 1) or reverse bias (the other state – logic 0), corresponding to a voltage change across the device of 1 volt. The different common modes were obtained by using the bias-T to shift each line equally. The nearly indistinguishable eye diagrams verify that the device is capable of receiving differential signals with a multitude of common mode voltages, rendering the same results and affording compatibility with different standards. In the 500mV amplitude symmetric tests 7dB extinction is obtained.

To obtain compatibility with LVDS we also demonstrate the performance with a 400mV swing on each line for a total of 800mV into the device in Figure 4. The common modes are the same. In the figures it is clear that the extinction degrades with lower voltage, however 5dB is still achievable.

Importantly, even though the measurements were performed with a bias tee (that is each side is AC coupled), the differential driving technique described here allows for DC-coupled operation with standard differential drivers of a variety of designs (LVDS, LV-CMOS, VML, CML). Additional testing at common mode voltages below 1V, compatible with current and future CMOS V_{dd}, also yielded eye diagrams that were indistinguishable from those shown.

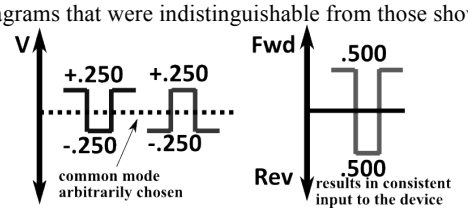

Figure 2 DC coupling of the device at three common modes. The common mode of the drive (dotted line) is varied from 250mV to 800mV to 1.2V always resulting in the same differential signal on the device.

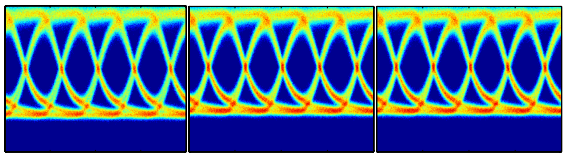

Figure 3 For 500mV drive eye diagrams for common modes of (left to right) 0mV, 1.25V and 1.5V show the same extinction verifying the flexibility of the device to DC couple at arbitrary voltage levels.

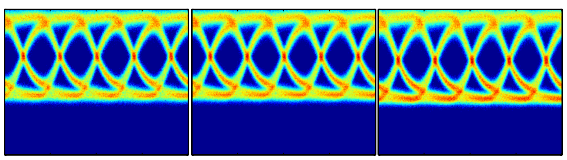

Figure 4 For 400mV the same common modes are shown for an extinction of 5dB. The voltage levels and amplitudes in these last three figures show compatibility with both CML and VML signaling.

IV. Energy per Bit

The energy per bit is calculated using the full amplitude of the voltage on device. The energy per bit has been measured using time domain reflectometry (TDR) in ½ volt increments. Additionally an analytical estimation of capacitance was obtained using the depletion approximation [8], which was supported by integrating the simulated charge movement in DAVINCI software from Synopsys. In particular, energy results are based on integrating the voltage over time in the case of TDR measurement, calculating the energy from $E=CV^2$ in the analysis, and integrating the charge over time in the simulations. In each case, the energy per bit is equal to the measured energy divided by 4, because the probability of switching from 0 to 1 is only ¼ of the total switching space (00 **01** 10 11).

Finding good agreement among the different methods we report the energy per bit values in the symmetric case to be 3.2fJ/bit for 1V swing (500mV drive amplitude) and 2fJ/bit for the 800mV swing (400mV drive amplitude signal).

V. Summary

Differential signaling into silicon photonic resonant modulators provides a promising method of realizing both the low voltage CMOS and low power drivers envisioned for enabling exascale computing. The symmetric drive capabilities demonstrated here are compatible with typical low voltage differential signaling techniques in that they have been tested with the same common mode voltages and voltage swings as common techniques such as LVDS, CML and VML. The modulator energy consumption was as low as 2fJ/bit with differential drive signal amplitudes of 400mV. The silicon modulators operate at 10Gbps with BER $<10^{-12}$ using 2^{31}-1 PRBS patterns.

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