Cryogenic Operation of Silicon Photonic Modulators

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Abstract: For the first time, simulation and operation of a silicon photonic modulator are demonstrated at cryogenic temperatures. The device operated at 5Gbps and 10Gbps at a temperature of 115K opening application areas in harsh environments.

OCIS codes: (130.3120) Integrated optics devices; (230.7390) Waveguides, planar.

1. Introduction

Recent demonstrations of ring and disk silicon micro-resonators continue to build the case for these devices as compact, low power and high-speed solutions for chip-to-chip optical interconnects [1-4]. These efforts have demonstrated very low power consumption (and energy-per-bit) as well as single volt drive which makes these devices compatible with current complimentary metal oxide semiconductor (CMOS).

Another area where bandwidth densities are increasing is focal plane arrays with the potential for megapixel arrays on orbital microscopes (the Kepler spacecraft has a 96 megapixel focal plane [5]). At this scale, detectors can produce data rates of terabytes requiring kilowatts of power with traditional electronic backplanes. Silicon resonant modulators can reduce this requirement to close to a Watt using recently demonstrated technology [3]. Furthermore, fiber based technologies are inherently resistant to electromagnetic interference and don't conduct heat which can further save power on cryogenically cooled arrays. In a controlled temperature environment, resonant devices also do not suffer channel drift as they would in traditional interconnect applications. This potentially removes the requirement for thermal tuning.

Here we demonstrate the first silicon resonant modulator to be cryogenically cooled to 115K and show that this technology performs comparably to devices operating at 300K. The results are supported with simulation based on the response of doped semiconductors in cryogenic environments.

2. Simulation and Modeling

The disk is fabricated using 250nm thick silicon on 3µm buried oxide. There is a 5µm deposited oxide over the device and waveguide. The P-type ohmic contact is approximately 100nm thick and the N-type is the full thickness of the silicon, and both ohmic contact regions are 2µm wide at the maximum. The depletion region is vertical and the 10^{18} cm^{-3} diode doping only covers π radians of the device. The design is fully described in [3].

The device operates in depletion mode using reverse bias. Carriers are swept out of the diode depletion region modulating the refractive index in a resonator coupled to a waveguide and tuned to an optical carrier frequency. In order to operate at high speed the effective resistance should be as low as possible. This is of particular importance in the p and n regions between the edge of the device and the contacts near the center of the device. Under cold temperatures and in reverse bias, the diode intrinsic region increases, effectively thinning the p and n regions, increasing the effective series resistance.

Simulations were performed to better understand the carrier ionization using custom software, and the results are shown in figure 1. The color map in the vertical plot shows the ionized carrier concentration as a function of the spatial dimensions of the device. The vertical junction of the device is represented by the y-axis along the direction of the bi-directional arrow with zero corresponding to the surface of the device and 0.2 corresponding to a depth of 200 nm into the device. The circular dimension of the device is approximated by the linear x –dimension along the front axis. The red vertical sections are the ohmic contacts. The carrier ionization in the p and n junction region of the active device is shown to be sufficient at 70K as shown in figure 1.

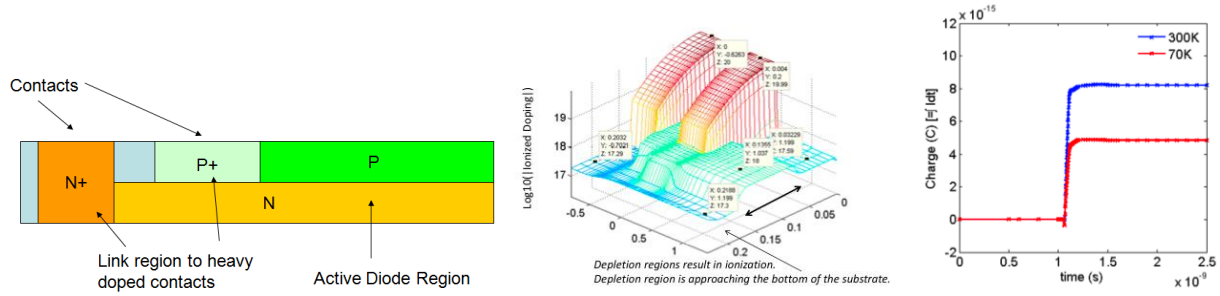

Figure 1: (Left) Schematic of the simulated device. (Middle) Simulation showing the carrier ionization of the device as a function of the spatial dimensions of the device. The z-dimension of our device is represented by the y-axis along the direction of the bi-directional arrow, and the circular dimension of our device is approximated by the linear x –dimension along the front axis. (Right) Time response of the charge distribution in the device, indicating adequate time response at cold temperatures for 10Gbps operation.

3. Device Operation at Cryogenic Temperature

The modulator was measured in a cryostat for both cold and room temperature operation. The cryostat had a pair of piezo-electric alignment stages to align lensed fibers to the edge of the device. A highspeed vacuum feed-through was used for RF signal. The experimental setup can be seen in figure 2. In initial optical experiments the device was not actively modulated, but only measured for resonant shifting due to temperature. Importantly, the resonance stays strong at cold temperatures shifting as expected but maintaining a quality factor of 10^4.

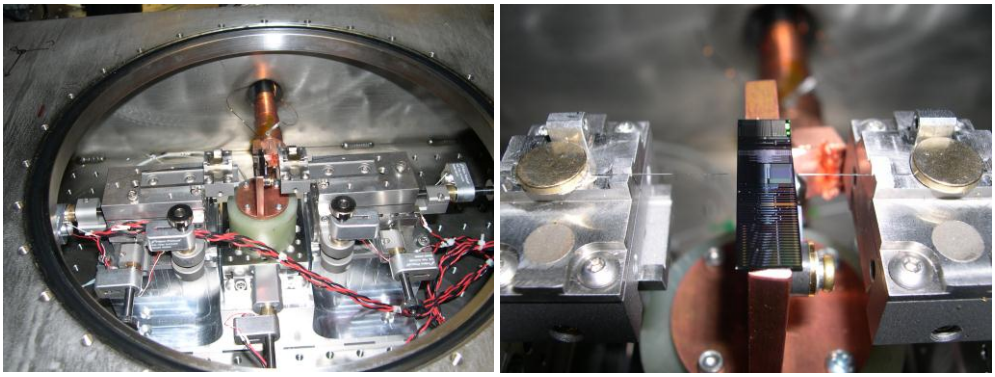

Figure 2: (Left) The optical characterization setup can be seen in the foreground of the cryostat. The piezo driven stages allow for the alignment of lensed fibers to the photonic chip in vacuum. The cold finger can be seen in the background, which is thermally coupled to the waveguide holder by copper braid. (Right) A detailed view of a photonic device being characterized by two lensed fibers in the cryostat.

The device was operated using 5Gb/s and 10Gb/s pseudo random data. Eye diagrams were measured and recorded at 300K and at 114K. At room temperature, the device was reverse biased at 1.3V, with a swing of 3.6V, for a voltage range of 0.5 to -3.1V. At cold temperature, the device was biased at 1.0V for a swing of 0.8V to -2.8V. The eye diagrams are shown below in figure 3. The eyes at room temperature are more open vertically, but they appear to have similar temporal responses. This better vertical eye opening could have been an artifact of having better optical coupling at room temperature. However, at low temperature the device has lower capacitance and moves less charge for a given voltage. This is an area of future work as we work to improve the operation of silicon photonics in cryogenic environments. In either case, the BER was ~ 10^{-9} at 5Gb/s with a 2^{31}-1 pattern and short-term low error rate (about 10^{-11}) with a 2^7-1 pattern. At 10Gb/s, the device error rate with a 2^7-1 pattern was about 10^{-4}. There is a significant increase to the noise by the addition of the nitrogen flow and vacuum pumping of the cryostat.

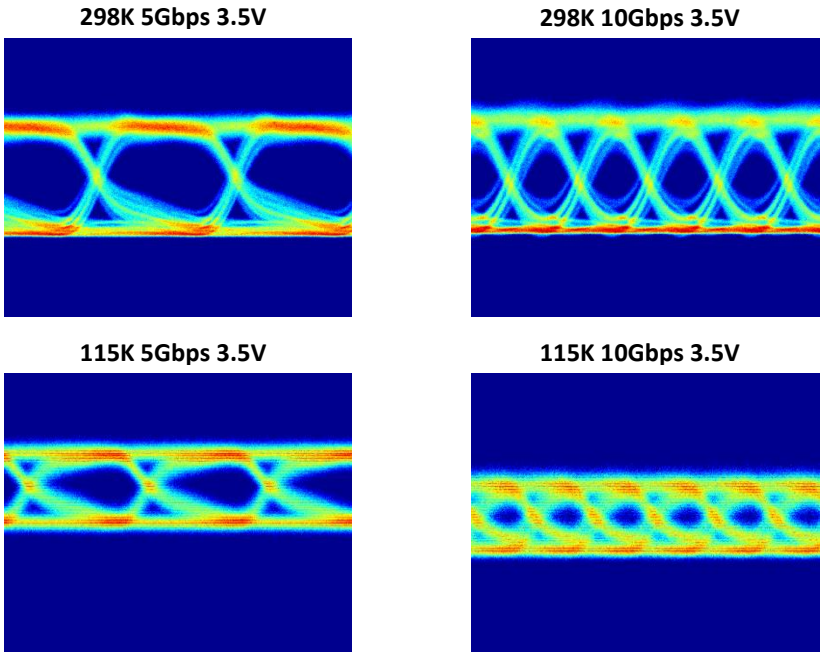

Figure 3: Eye diagrams of the silicon photonics modulator at 115K and at room temperature. The eye has better vertical opening at room temperature but remains open at 115K. The increased noise is due to a decrease in optical coupling and significant vibrations due to operating in a cryostat.

4. Conclusions

To our knowledge, this is the first investigation of silicon photonic modulators operating at cryogenic temperatures. This opens up a new field of applications for these devices to operate as backplanes on focal plane arrays and other areas where cooled detectors or cryogenic operation of computing is done. In this work, we have described simulations and operation of a silicon photonic modulator for focal plane array communications at cryogenic temperature of 115K. The device performed well at 5Gbps and maintained an open eye at 10Gbps at low temperature.

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5. References

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