Integration of Silicon Photonics in a Bulk CMOS Memory Flow

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***ABSTRACT* – Monolithically integrated silicon photonic (SiP) devices have been demonstrated using a modified bulk CMOS flow. Integration was achieved by nominally extending existing process and design collateral without shifting the CMOS parameterization.**

***KEYWORDS*– bulk CMOS; optical interconnections**

I. INTRODUCTION

The latest incarnation of double data rate synchronous dynamic random-access memory, DDR4, is expected to reach per pin rates as high as 3.2 Gbps. However, expanding beyond these rates is challenging, since signal integrity is a concern even for DDR4. In addition to signal integrity, energy, bandwidth, and cost must be considered. In the industry, there is interest in alternative electrical [1] and optical solutions [2,3] for chip-to-chip interconnects. However, given the historical price sensitivity of DRAM, and memory products in general, it is reasonable to assume that any interconnect for memory products must deliver performance improvements while remaining cost-efficient. This paper presents work towards that goal, outlining the monolithic integration of SiP devices on a bulk CMOS process.

II. MONOLITHIC INTEGRATION

A. Objective

The project's objective is the demonstration of a cost-efficient optical interconnect on a memory process flow. In order to achieve this, one must rely on the existing CMOS platform, remain within the process flow's thermal budget, and minimize cost through the reuse of existing steps. The resultant motif drove the project towards Front-End-of-Line (FEOL) focused integration on a triple level metal bulk CMOS memory process.

B. Process Development Kit

The Computer Aided Design collateral was modified and augmented to support the project. The collateral includes a full Design Rule Manual, design rule checks, mask generation flow, and Optical Proximity Correction (OPC). Fig. 1 shows an example OPC structure. Note that the curved optics were fabricated in a process that only allows for orthogonal lines, adding to the challenge. While additional features need to be implemented, a working Process Development Kit (PDK) has been established.

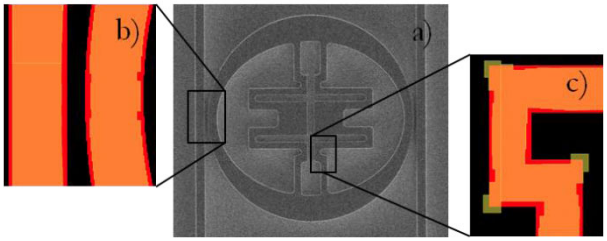

Fig. 1. (a) Planar micrograph of an example Adiabatic Ring Modulator (ARM) with integrated heater, drawn (red) and Optical Proximity Corrected (yellow) (b) waveguide to ring gap, and (c) local interconnect detail.

C. Process Integration

The project has been FEOL-centric with a focus on process reuse. An example of reusing existing layers is the selection of the CMOS gate polysilicon stack as the waveguiding layer. This decision enabled the fabrication of cost effective SiP structures, at the expense of higher waveguide attenuation and increased process integration challenges. Existing implants, dopant activation, and device patterning processes were used. However, a zero process change SiP project [4] was not viable.

When necessary, additional processing steps were added to the standard process flow. Given the

This work was funded in part by DARPA award HR0011-11-9-0009. The views expressed are those of the authors and do not reflect the official policy or position of the Department of Defense or the U.S. Government.
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proximity of the waveguides to the bulk CMOS substrate, additional "bottom cladding" was needed. A Deep Trench Isolation scheme was developed for the SiP devices, see Fig. 2. The introduction of this high volume manufacturing compatible processing enables SiP on bulk CMOS.

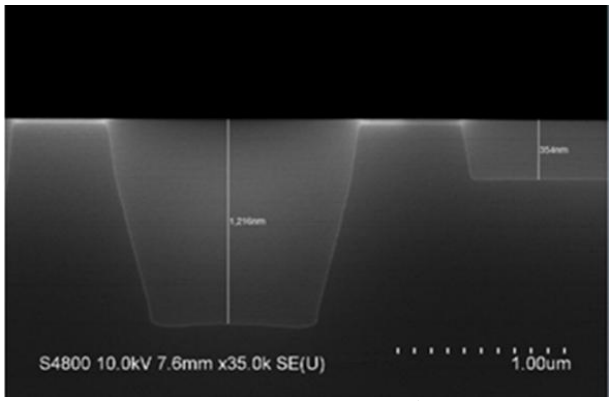

Fig. 2. Cross section micrograph showing adjacent Deep Trench Isolation (DTI) and Shallow Trench Isolation (STI). DTI enables fabrication of FEOL waveguides without undue coupling to the substrate, while the standard STI is used for the standard CMOS.

Another significant process modification was the inclusion of a partial polysilicon etch. As shown in Fig. 3, this etch enables improved vertical couplers. The combination of a DTI and the vertical couplers facilitates wafer level testing, a requisite technique for process improvement and monitoring.

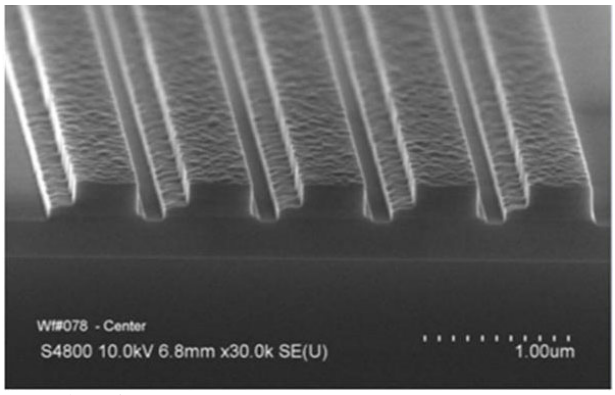

Fig. 3. Angled cross section micrograph showing an example vertical grating coupler fabricated by full and partial thickness polysilicon etches. Note etch profile and surface roughness.

III. Results

A. CMOS Performance

The integration of SiP did not significantly alter the CMOS performance. End-of-line parametric and functional testing has been confirmed. This allows for the reuse of the preexisting SPICE models.

B. Waveguide Attenuation

An expected consequence of using polysilicon as the waveguide media is higher attenuation. In fact, average end-of-line bulk loss for the polysilicon waveguides was 18 dB/cm, see Fig. 4. While high when compared to SOI based implementations, one must balance the competing performance and cost constraints. If one were focused on providing optical interconnect to a DRAM die, the tradeoff between process cost and performance may be acceptable. Additionally, waveguide attenuation could be reduced with confinement factor optimization and general process improvements.

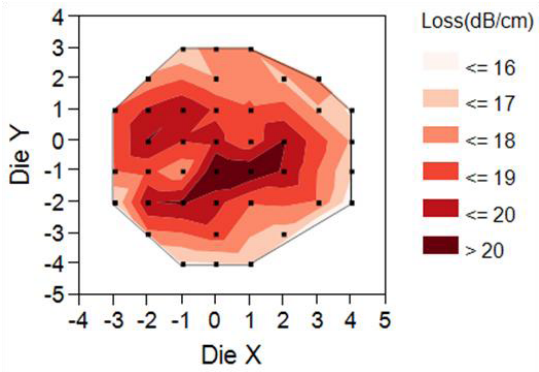

Fig. 4. Polysilicon waveguide bulk loss at 1280 nm measured on a single end-of-line 200 mm wafer. The attenuation ranged from 15 dB/cm to 21 dB/cm with a sample size of 40.

IV. Conclusion

The monolithic integration of SiP structures on a bulk CMOS process has been demonstrated. A functional PDK and process flow have been developed. Future work will focus on the development of active SiP elements, improved passive device performance, and packaging.

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