Integrated Microring Tuning in Deep-Trench Bulk CMOS

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Abstract: An all-digital ΔΣ-based heater driver and a 6-µm diameter microring resonator are monolithically-integrated in deep-trench bulk CMOS. With clock scaling and 2.5V supply voltage, the system demonstrates a 350GHz tuning range and 10-15µW/GHz tuning efficiencies.

1. Introduction

Wavelength-division multiplexed (WDM) silicon-photonic links form a promising alternative to tradional electrical interconnects. However, the essential component of these WDM networks, the microring resonator, suffers from resonance drifts due to either static process variations or dynamic temperature fluctuations, necessitating methods for active resonance tuning [1]. Thermooptic tuning can be accomplished through over-clad heaters [4,7,8] or silicon heaters directly integrated into adiabatic resonator microrings (ARM) [1,3,5,6]. Unfortunately, thermal tuning can consume a significant portion of the overall link power budget [2], motivating device and system design to characterize and improve thermal tuning efficiency. To date, this concept has been demonstrated and characterized for devices built on thick SOI with and without localized substrate removal (undercut) [3-5], in thin SOI with silicon-carbide substrate transfer [7], and in bulk CMOS with localized substrate removal under shallow-trench isolation (STI) [8].

In this work, we demonstrate a heater driver system for microring resonators consisting of a fully-digital ΔΣ-based heater driver circuit and an ARM filter (Fig. 1, left), both monolithically integrated in a commercial 0.25 µm-equivalent bulk CMOS process with deep-trench isolation capability. Integration of the heater driver alongside the integrated heater minimizes the parasitic resistance from driver to the heater, provides a digital heater control interface through which multiple rings can be controlled on-chip, and eliminates the dedicated pads for external heater control used in the majority of previous work. Using a process-compatible supply voltage of 2.5V, the system is able to tune the resonance of an ARM filter by 350GHz, with an efficiency of 10-15µW/GHz.

2. System Overview

The driver circuit consists of a synthesized pipelined accumulator and a custom one-transistor driver head (Fig. 2, right). The circuit utilizes pulse density modulation (PDM) to output a heater drive waveform consisting of a digital pulse train, with a duty-cycle corresponding to an 8-bit digital input setting. The slow thermal response of the ring heater smoothens ripples in temperature and transmission introduced by the digital nature of the drive waveform, provided that the driver's clock frequency (and hence the PDM's oversampling ratio) is set significantly higher than the thermal time constant. Since power consumption of the circuit scales with the clock frequency, driver power can be optimized by fine-tuning the oversampling ratio of the PDM. The duty-cycled nature of the driver guarantees a monotonic and linear relationship between heater power and input setting, as well as constant step size. The implementation in this work is aggressively pipelined to hit frequency targets >400MHz and sized to drive >5mA of current. Design constraints can be relaxed to lower driver power and area.

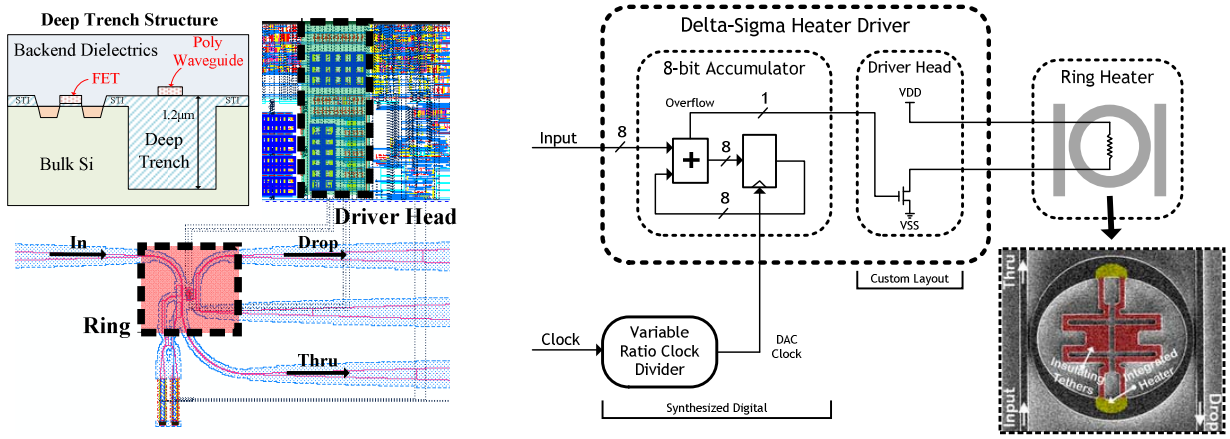

Figure 1 – Layout of the integrated heater driver connected to the ARM filter, both integrated in a deep trench CMOS process (left). Block diagram of the ΔΣ-based heater driver with SEM of the connected ARM filter (right). The ARM filter, 8-bit accumulator, and driver head occupy 28µm^2, 1500um^2, and 2500 um^2 of area, respectively, including area used for decoupling capacitances and fill cells.

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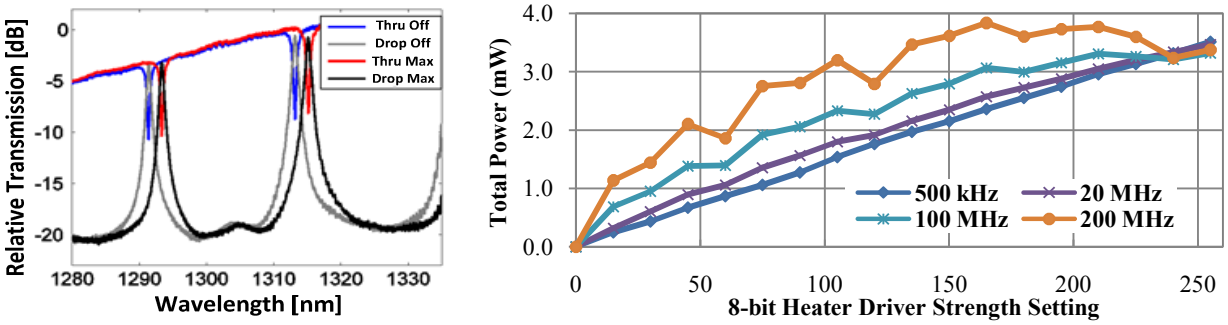

Figure 2 – Optical transmission vs. wavelength when driver is off and at max power (left) and total power consumed at various driver power settings (right). For reference, *off* corresponds to a driver strength setting of 0, *max* corresponds to a strength setting of 255.

The ring and circuit are integrated in a deep-trench bulk CMOS process (equivalent to a DRAM periphery process), with Poly-Si waveguides above deep oxide trenches (Fig. 1, left). The 6-μm diameter ARM filter [6] is designed to work at a wavelength of λ~1290nm with a deep-trench. The single-mode waveguide width is 280nm in the coupling region and adiabatically tapered to 600nm to allow contacts to the adiabatic region. Single radial mode propogation is preserved through the adiabatic region, achieving an uncorrupted free spectral range (FSR) of 3.7THz (Fig. 2, left). The integrated heater with a resistance of ~1.7kΩ is formed by *n* type doping in the adiabatic region and the Si-tethers are doped *n*+ with silicide to minimize contact resistance and to insulate the tethers (Fig. 1, right-inset).

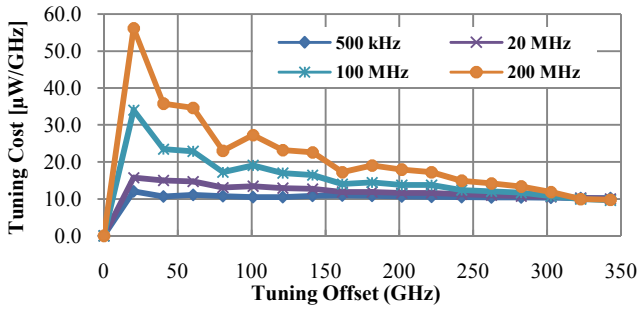

Figure 3 – Tuning cost per gigahertz, with driver cost included, to reach a specific tuning offset

Process	Raw Cost	FSR	Normalized
Bulk deep trench (this work)	10 μW/GHz	3.7 THz	37.0mW/2π
Thick SOI [3]	42.2 μW/GHz	1.6 THz	67.4mW/2π
Thick SOI with undercut [4]	1.67 μW/GHz	1.4 THz	2.34mW/2π
Thick SOI [5]	4.4 μW/GHz	5.6 THz	24.6mW/2π
Thin SOI with substrate transfer [7]	14.3 μW/GHz	2.04 THz	29.2mW/2π
Bulk shallow-trench with undercut [8]	2.9 μW/GHz	4.0 THz	11.6mW/2π

Table 1 – Comparison of the tuning costs between this work at 20 MHz in the high power regime and other works. The normalized cost is calculated as (Raw Cost) × (FSR/2π).

3. Measurement Results

The heater output power is 3.5mW at the *max* power setting, limited by supply voltage (2.5V) and heater resistance (1.7kΩ). We achieve a maximum resonance shift of 350GHz (Fig. 2, left), corresponding to a step size of ~1.37GHz for an 8-bit input. Compared to the power delivered to the ARM's heater, the power overhead for the driver circuit is negligible at a clock frequency of 500kHz but substantial at 200MHz (Fig. 2, right). The tuning cost of the system improves with higher tuning offsets (Fig. 3), as the relative power overhead of the driver circuit shrinks compared to the power going to the heater. For the fabricated ARM filter, a clock frequency of 20MHz provided sufficient oversampling to minimize the transmission ripples, leading to a tuning cost between 10-15μW/GHz.

3. Conclusion

We demonstrated a monolithically-integrated heater driver system in a commercial bulk CMOS deep-trench process. We achieved a 350GHz thermal tuning range and 10-15μW/GHz tuning for an ARM. To the best of our knowledge, this is the first demonstration of ring thermal tuning and efficiency optimization in a deep-trench bulk process.

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