Vertical Junction Silicon Microdisk Modulators at 25Gb/s

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Abstract: We demonstrate the first vertical junction microdisk modulator to achieve an open eye diagram at 25Gb/s. The result was achieved using a circularly contacted microdisk with a 3μm radius and a 1.2V_{pp} drive for ~13fJ/bit.

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1. Introduction

High-performance computing systems require need high bandwidth, low power, and scalable optical interconnects to maintain balanced communications in future exascale machines. Low power, low voltage, high speed, and compact CMOS compatible silicon electro-optic modulators are key enablers for next generation optical interconnects. Silicon modulators based on the free-carrier effect in silicon [1] achieve high-speed modulation by injecting [2] or depleting charge [3,4] inducing a frequency shift in a Mach-Zehnder interferometer or resonant device that translates the resultant frequency shift into an amplitude response. Resonant modulators confine light in compact high-Q devices enhancing the interaction of the light with the change in charge distribution. Compact resonant devices also minimize the device capacitance, enabling high-speed and low power modulators [5-10]. The first resonant modulators utilized carrier-injection in a *p-i-n* junction and ridge-waveguides for electrical contacts [5-10]. However, carrier injection based devices are bandwidth limited by the free-carrier lifetime in silicon and ridge-waveguides with external electrical contacts increase the device size, and Free-Spectral-Range (FSR), due to the increased minimum bend-radius induced by radiation through the silicon ridge layer. Further, while ridge waveguide based modulators work well in injection configurations, in depletion-based modulators, the lateral *p-n* junctions that have been employed exhibit a poor overlap with the optical mode, resulting in excess losses, higher drive voltages, and/or reduced extinction [10]. Centrally contacted microdisks [6-9] and microrings [9], with vertical *p-n* junctions and a hard outer resonator wall substantially increase the overlap of the optical mode with the depletion region thereby reducing the drive voltage, improving the extinction and reducing the excess losses, while simultaneously greatly reducing the device size, capacitance and power consumption. In record-setting demonstrations, vertical *p-n* junction devices have achieved error-free modulation up to 12.5Gb/s with only a 1V drive and while consuming only 3fJ/bit [7,8]. However, to date, vertical junction modulators have been limited to 12.5Gb/s [7-9]. Here, we present the first vertical junction modulator to achieve open-eye diagrams up to 25Gb/s.

Previous demonstrations of vertical junction silicon modulators were limited by excess device resistance and capacitance caused both by design and non-Ohmic electrical contacts [6-9]. To reduce the resistance in the device we devised a circularly contacted silicon microdisk modulator (Fig. 1). The circular contact ensures that the electrical path out to the junction is effectively both short and wide, therein minimizing resistance.

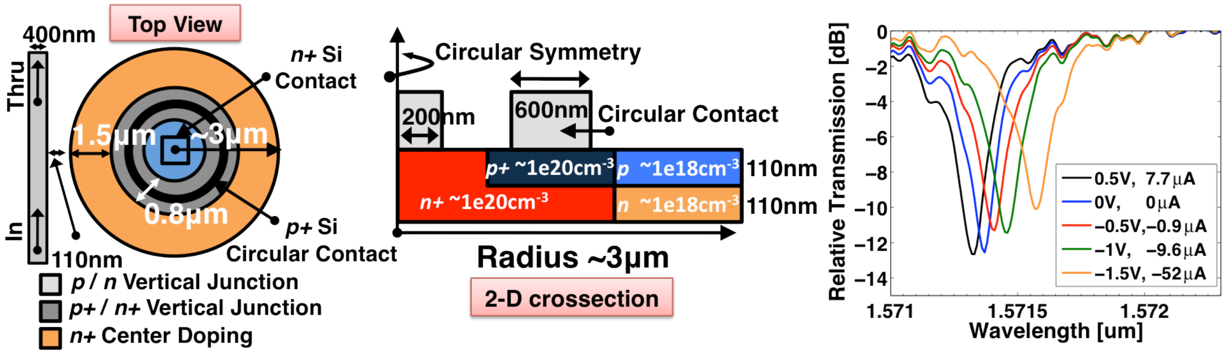

Fig. 1. (left) Top-view of the 6-μm-diameter microdisk modulator which utilizes circular inner contacts. (middle) 2D crossection showing the doping profile with *p-n* and *p+/n+* vertical junction. (right) Spectral response of the microdisk modulator with respect to voltage dropped and current passing through the junction.

The ~3μm radius microdisk modulator has a hard outer wall to maximize confinement and minimize optical bend loss and *n+* and *p+* doped regions with a carrier concentration $\sim 1\times10^{20}$ cm^{-3} to minimize the resistance out to the $\sim 1\times10^{18}$ cm^{-3} doped *p-n* junction. The *p-n* vertical junction, centered ~110nm thickness, is chosen to maximize the mode overlap and formed around the edge (annulus of ~1.5µm) to have low carrier absorption. The *p+/n+* junction is formed inside the microdisk where it is invisible to the fundamental radial mode, to allow a low resistance circular *p+* contact and central *n+* contact which will minimize the resistance of the overall device (Fig. 1 left-middle). The modulator was fabricated by using 193-nm immersion lithography on a 220 nm thick silicon-on-insulator (SOI) wafer with 2µm buried oxide (BOX) layer for optical isolation. The center contact is a 0.4µm×0.4µm square and the annulus of the circular contact is ~0.6µm wide. The microdisk is optically fed by a single mode, 400nm wide input waveguide with a 110nm coupling gap designed to ensure critical coupling.

2. Measurements and Analysis

A GSG probe was landed to apply a voltage across the junction. Spectra were measured for a voltage sweep from +0.5V to -1.5V (Fig. 1 right). The voltage range was chosen to keep the diode off and in depletion mode. To maximize extinction ratio for an AC measurement, an AC coupled 1.2V_{pp} was chosen as the device operating voltage when using a 50Ω terminated GSG probe. For a high impedance termination, only 0.6V_{pp} is required.

In order to characterize the modulators and electro-optic test bench is used. An input tunable CW laser source was aligned with a polarization controller for TE excitation of the bus waveguide and the resonance of the microdisk modulator at ~1571.4 nm. The electrical data generated by a pattern generator, is a non-return-to-zero (NRZ) on-off-keyed (OOK) signal, encoded with a 2^{31}–1 pseudo-random bit sequence (PRBS). An electrical amplifier was used to achieve an AC coupled 1.2V_{pp} drive signal at the desired data rates. Drive voltage is applied to the modulator with a 50Ω-terminated GSG probe and the voltage dropped across the modulator is also ~1.2V_{pp}. The optical thru port is then received by an Erbium Doped Fiber Amplifier (EDFA) to overcome fiber-to-chip coupling losses and a tunable bandpass filter with a 1nm 3dB bandwidth, was used to filter out the Amplified Spontaneous Emission (ASE) of the EDFA. Eye diagrams were then taken with a sampling scope at data rates of 10Gb/s, 15Gb/s, 20Gb/s, and 25Gb/s (Fig. 2). The dynamic extinction ratio and insertion loss based on the optical eye diagrams are summarized in Fig. 3. With low insertion loss (~1dB) and high extinction ratio (>6.9dB), the measurements are comparable to commercial modulators. As can be seen from the eye-diagrams, the eyes are wide-open all the way up to 25Gb/s.

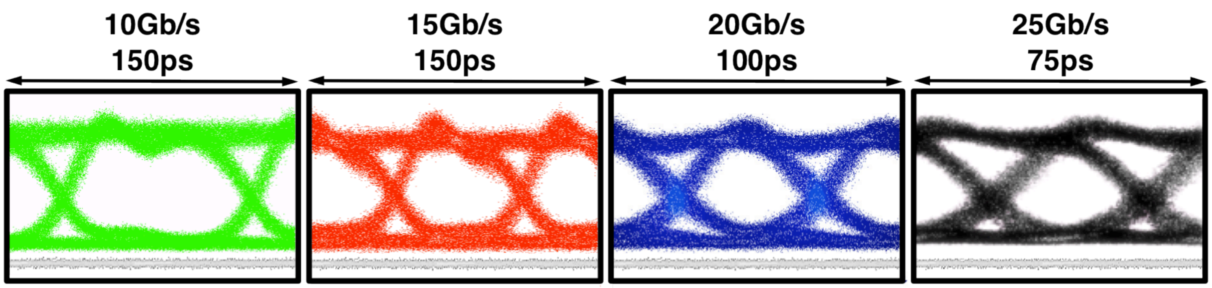

Fig. 2. Measured optical eye diagrams from the on-chip silicon microdisk modulator at AC coupled device voltage of 1.2Vpp at 10-, 15-, 20-, 25-Gb/s data dates. The eye diagrams are shown with the true zero (gray line) at each data rate. The true one level is obtained by setting the laser off resonance by ~1nm and decreasing the EDFA to a non-satured level. The true one level can be calculated using the Fig. 3 insertion loss data.

For Bit-Error-Rate (BER) testing, a variable optical attenuator (VOA) was inserted before the receiver placed to adjust the received power level. The optical data was detected by a high-speed *p-i-n* photodiode and transimpedance amplifier (PIN-TIA) receiver and fed to the Bit-Error-Rate Tester (BERT) differentially for evaluation. No pre-emphasis or equalization was used throughout the experiments. The total fiber-to-fiber insertion loss was ~16.5 dB. A commercial lithium niobate ($LibNO_3$) Mach-Zehnder modulator was substituted in for the on-chip microdisk modulator for comparison and power penalty. The commercial modulator is rated at 35GHz 3dB bandwidth, and driven with an AC coupled voltage 5.5V_{pp} electrical signal.

In order to further quantify modulator performance, BER measurements and power penalty analysis is performed from 10Gb/s to 25Gb/s data rates (Fig. 4). For up to 20Gb/s, we have error free operation (BER <10^{-12}). At 25Gb/s even the commercial modulator cannot perform error free operation for the current setup parameters. Therefore, we believe the BER is limited by the experimental setup rather than the device itself. The power penalty is the relative received power difference at a BER of 10^{-9} between the silicon microdisk modulator and the commercial modulator (Fig. 4). Data transferred by the silicon microdisk modulator have received with a positive power penalty of 0.29, 0.68, 1.17 and 2.06 dB, at data rates of 10Gb/s, 15Gb/s, 20Gb/s and 25Gb/s, respectively.

We can estimate the modulator energy-per-bit of the microdisk modulator (E_M) by calculating the average junction capacitance (C_J) and using the experimental voltage swing (Vpp); E_M=$CV_{pp}^2/4$ [6,7]. The junction capacitance is $C_J=\varepsilon_0\ \varepsilon_{Si}A/d$ where, ε_0 is vacuum permittivity, ε_{Si} is relative permittivity of Si, A is junction the area and d is the depletion width. Sentaurus simulations are performed to estimate average depletion width and determined as ~65nm which leads to a junction capacitance of ~35fF. For a 1.2V_{pp} drive voltage the modulator energy-per-bit is ~13fJ/bit.

Data Rate	Extinction Ratio [dB]	Insertion Loss [dB]	Power Penalty [dB]
10 Gb/s	9.22	0.45	0.29
15 Gb/s	8.57	0.65	0.68
20 Gb/s	7.6	1.12	1.17
25 Gb/s	6.9	1.59	2.06

Fig. 3. Summary of the demonstrated results of the silicon microdisk modulator for data rates from 10Gb/s to 25Gb/s. Extinction ratio and insertion loss is based on the optical eye measurements. The measured power penalty of microdisk modulator is relative to the commercial lithium niobate modulator.

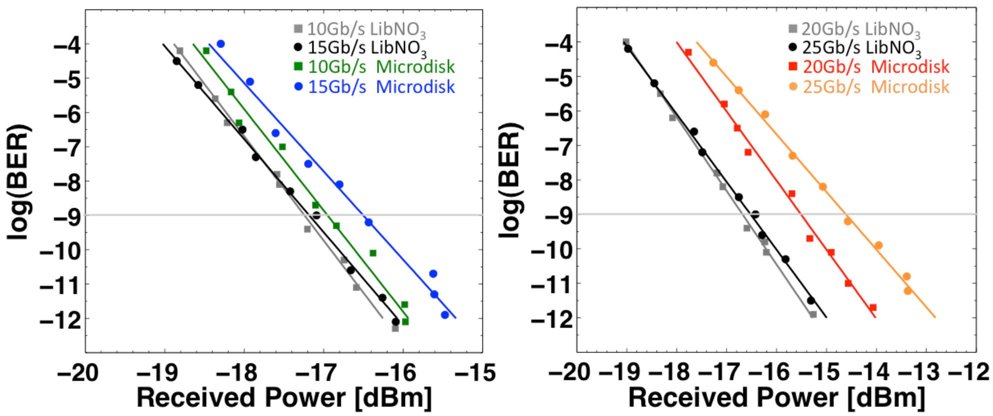

Fig. 4. Bit-error-rate (BER) curves measured for microdisk modulator. BERs are experimentally measured for data rates at 10Gb/s, 15Gb/s (left) and 20Gb/s, 25Gb/s (right). The results are compared to a lithium niobate Mach-Zender modulator and power penalty is obtained relative to this modulator.

3. Conclusions

We demonstrate the first vertical junction silicon microdisk modulator to achieve open eye-diagrams at a data rate of 25Gb/s and error-free operation up to 20Gb/s. These high-speed results were enabled by a unique doping profile which circularly contacts the modulators to reduce the device resistance while maintaining a hard outer wall for maximizing the optical confinement. The device represents the smallest silicon modulator to run at 25Gb/s and achieves the lowest reported power penalty, important for the overall power budget in a microphotonic link.

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