Ultralow Power Silicon Modulators

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Abstract: We discuss recent results in low-energy (0.9fJ/bit) high-speed (25Gb/s) electro-optically stabilized microdisk modulators. The combined results of highly efficient modulation and electro-optic thermal compensation represent a major step towards single-digit femtojoule-class communications. ©2014 Optical Society of America

OCIS codes: (130.3120) Integrated optics devices; (230.5750) Resonators; (230.7370) Waveguides

1. Introduction

Silicon photonics has been developed as a platform for low-power high-bandwidth communications, and the many impressive results on modulators [1-4], filters [5], and detectors [6], have produced considerable interest in the field for addressing the bandwidth and power consumption limitations within high-performance computers, data centers, and even on-chip communications. Yet, on-chip (i.e. intra-chip) communication links, where the bandwidth and efficiency requirements are far more severe, an interconnecting wire that communicates one bit over an average distance on-chip of 1mm (~10% of the die size), consumes 100fJ/bit [7]. At the 8nm node and beyond, over one petabit-per-second of data transfer will be required on large microprocessor die, leading to 100W of communications power per chip (nearly ten times what is acceptable in practice), and providing a clear motivation for on-chip photonic interconnects to be driven into the single-digit femtojoule-per-bit regime with each component within the link consuming just a fraction of that total [7-8]. Yet, despite years of development, silicon modulators have struggled to achieve simultaneous low power and high-speed operation. Additionally, low power resonant structures, must be thermally controlled, an approach that has led to dramatic increases in power consumption [9].

Here, we present the design and demonstration of an athermal resonant silicon modulator that is compatible with a complementary metal-oxide-semiconductor (CMOS) process, that simultaneously operates at high data rates (25Gb/s) while achieving sub-one-femtojoule-per-bit (0.9fJ/bit) operation [4]. These results are made possible by combining interior circular contacts and a highly optimized vertical junction within a compact microdisk modulator (Figure 1). The circular contacting scheme enables a direct, short electrical path out to the vertical junction, minimizing the device resistance and thereby maximizing the depletion/accumulation response and the speed of the modulator. The vertical junction profile maximizes capacitance-per-unit volume, which is a figure of merit for electro-optic modulators. As a result, we achieve a record 250pm/V (30GHz/V) electro-optic frequency response and, thus, simultaneous error-free, high-speed (25Gb/s), low-voltage (0.5V_{PP}) and low energy-per-bit (0.9fJ/bit) operation. Further, the record electro-optic frequency response can be used to counteract thermal shifts over a 10°C (~100GHz) temperature (frequency) range by varying the DC bias point of the modulator and consuming only 2.77fJ/bit in total (Figure 2).

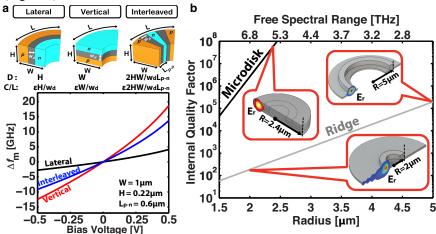


Figure 1- a. Lateral, vertical and interleaved junction profiles for common depletion-mode modulators. The capacitance per unit length (C/L) is expressed below each junction profile. The frequency shift as a function of bias voltage for three different junction profiles, showing the large frequency shift of vertical junction profile. Calculations were performed for λ =1.55 μ m and a fixed core thickness of 220nm, width of 1 μ m, p-n junction length of 600nm, a built-in potential of 0.7V, and a n- and p-type carrier concentration of 3×10^{18} cm⁻³. b, The internal quality factor as a function of radius for a microdisk and ridge resonator. TE radial electric field mode profiles of important points are overlaid with the resonator cross-sections. (reproduced from [3])

Finally, while these demonstrations were all performed at 25Gb/s, the modulator demonstrates open eye-diagrams at data rates as high as 44Gb/s when driven with higher voltages.

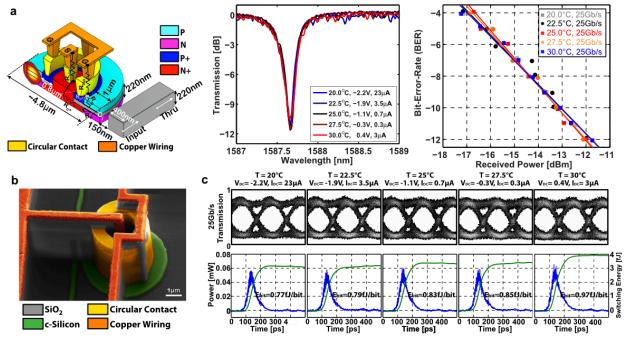


Figure 2- a, A 3D sketch of the electro-optic silicon microdisk modulator, showing the cross-section, size, doping profile, metal connections and the optical mode overlapped with the vertical p-n junction. b, A scanning electron microscopy image of the silicon microdisk modulator, revealed by dry etching the SiO₂ around the modulator. c, The measured transmission spectra of the resonator over a 10°C temperature range with the modulator tuned electro-optically to compensate for thermal variations. The bit-error-rate curves, showing error-free operation and measured over a 10°C temperature range for the silicon resonant modulator, which is driven with a terminated probe and 0.5V_{PP} NRZ-OOK PRBS with a pattern length of 2^{31} -1 at a data rate of 25-Gb/s. The power penalty due to temperature variations is within \pm 0.05dB. Experimentally measured high-speed optical eye diagrams of the silicon electro-optic modulator at 25-Gb/s. The applied bias voltage (V_{DC}) and measured current (I_{DC}) are denoted above the eye diagrams at each temperature. The extinction ratio (ER) and insertion loss (IL) are denoted below the eye diagrams at each temperature. The time domain reflectometer measurements of the electro-optic modulator energy consumption and switching energy for a 0.5V_{PP} drive for the indicated DC-bias voltages. (reproduced from [4])

2. Conclusions

We demonstrated the lowest power modulator (0.9fJ/bit) in silicon to date at a data rate of 25Gb/s. The resonant device operated over a 10°C temperature range in an athermal fashion utilizing low power electro-optic tuning, and consuming a total energy of only 2.77fJ/bit. The combined result improves upon the overall energy consumption of modulators by nearly two orders of magnitude. Yet, these results represent only the beginning of electro-optic control of the resonant frequency. With their efficient, 0.9fJ/bit operation at the increasingly important 25Gb/s data rate, and with the effective elimination of heater power consumption, these results represent an important first step towards achieving femtojoule-per-bit class communication links that will prove critical for future on-chip applications.

This work was supported in part by the Defense Advanced Research Projects Agency (DARPA) Microsystems Technology Office's (MTO) POEM and E-PHI programs.

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