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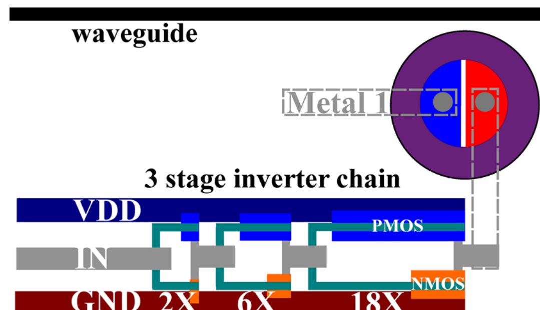
William A. Zortman
Douglas C. Trotter
Anthony L. Lentine
Gideon Robertson
Alex Hsia
Michael R. Watts



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Monolithic and Two-Dimensional Integration of Silicon Photonic Microdisks With Microelectronics

William A. Zortman,[1,2] Douglas C. Trotter,[1] Anthony L. Lentine,[1] Gideon Robertson,[1] Alex Hsia,[1] and Michael R. Watts[1,3]

[1]Applied Photonic Microsystems, Sandia National Laboratories, Albuquerque, NM 87185 USA
[2]Center for High Technology Materials, University of New Mexico, Albuquerque, NM 87185 USA
[3]Research Laboratory of Electronics, Massachusetts Institute of Technology, Cambridge, MA 02139 USA

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Abstract: A low-power silicon photonic disk resonator is monolithically and two-dimensionally integrated with complementary metal–oxide–semiconductor (CMOS) electronics. The results show direct integration with established CMOS manufacturing lines without changing either the CMOS or the photonic process stack. Comparable results for each integration method show subpicojoule per bit modulation and the potential for further reductions. The analysis reveals that the process of integration does not limit the performance of photonic or electronic components, and clear steps to use smaller drivers to achieve sub-50 fJ/bit at 10 Gb/s operation are available.

Index Terms: CMOS, monolithic integration, 2-D integration, silicon photonic devices.

1. Introduction

Many silicon photonic devices with high bandwidth and low power have been demonstrated recently [1]–[12]. For the most part, these are compatible with high volume manufacturing in silicon through hybrid integration using chip bonding [13]–[15], backend integration within a complementary metal–oxide–semiconductor (CMOS) process [16], or otherwise monolithically in the front end of the process [17]. The intent is close integration of optical communication devices with the silicon CMOS platform in order to provide high bandwidth/low energy interconnect for future multiprocessors, high performance computers and data centers [18]–[20].

Other groups have done demonstrations of integration of photonics with electronics using silicon and other substrates as noted above. In this paper, we demonstrate 2-D integration and monolithic integration of silicon photonics and electronics where the on chip electronics drive the modulator. It is noteworthy that no change to the standard CMOS process was required. This "drop-in" capability highlights the advantage of silicon photonics over other optical interconnection technologies, such as vertical cavity surface emitting lasers (VCSELs), for integration with existing high volume manufacturing CMOS operations.

Two concepts are demonstrated, 2-D wire bonding and monolithic integration. Two-dimensional integration means that the discrete chips sit side by side as opposed to 3-D integration where the

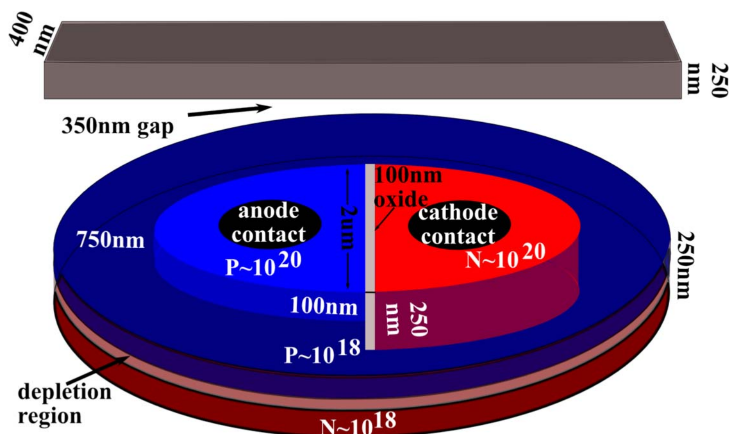

Fig. 1. Three-dimensional representation of the 3.5-μm diameter disk resonator, which is fabricated using 250-nm-thick silicon on 3-μm buried oxide. There is 5 μm deposited oxide over the device and waveguide. The P-type ohmic contact is approximately 100 nm thick, the N-type is the full thickness of the silicon, and both ohmic contact regions are 2 μm wide at the maximum. The integrated device adds a 100-nm oxide strip to reduce capacitive coupling between the ohmic contacts.

parts are stacked. The 2-D demonstration uses a Sandia designed and manufactured silicon photonic chip wire bonded to a standard IBM 90-nm CMOS driver. The second approach is a monolithic integration of the same photonic device with an inverter chain that drives the photonics. The two schemes are useful for comparison and also demonstrate two potential uses for integrated photonics and electronics.

2. Discrete Photonic Device

The photonic device is fabricated in 250-nm-thick silicon on 3-μm buried oxide using a 0.35-μm process on 6-in silicon-on-insulator (SOI) wafers. This is the standard process used on Sandia's Microelectronics Development Lab (MDL), which is an active manufacturing line that also runs application specific integrated circuit (ASIC) parts for numerous terrestrial and space applications and as such the products are radiation hardened (RADHARD). The photonic device that we integrated is shown in Fig. 1 and has been described in detail in [6]–[8]. Interested readers can find a scanning electron microscope (SEM) in [7]. The device is 3.5 μm in diameter with 0.5 μm tungsten filled contacts connecting to a metal 2 interconnect, which is 2 μm above the surface of the silicon. The contact liners are titanium, which are silicided $(TiSi_2)$ to $10^{20}/cm^3$ doped P and N ohmic contact regions. These regions are separated from each other by 100 nm of filled oxide trench in the monolithic application discussed below. There is a vertical PN junction in the periphery doped to $10^{18}/cm^3$ with N-type dopants on the bottom and P type on the top. The peripheral PN junction limits the junction capacitance resulting in higher speed. The device is optically coupled to a 400-nm-wide bus waveguide across a 350-nm gap in the coupling region. There are 10 μm of deposited oxide covering the silicon, and there is 3 μm of buried oxide underneath the silicon.

The device performance in its discrete form is shown in Fig. 2. The DC plot shows $\sim$10 dB extinction, and if the laser line is at the zero detuning point, then 1-dB insertion loss is seen above and beyond the waveguide loss off resonance. When coupling on/off chip there is a total 20-dB loss when using lensed fibers. The Q is about 10^4. Fig. 2(b) shows that this device can achieve 7 dB extinction using a 3.5-V drive voltage at. This is achievable with the device electrical 3 dB BW of 6 GHz, limited mainly by the series resistance of the diode. The bit error rate is $< 10^{-12}$. The discrete performance is shown here for comparison to the integrated devices. The energy consumed per bit is about 50 fJ/bit at 3.5 V if pad capacitance is not taken into account.

As described in [6]–[8], this device exists in a 50% doping configuration and has been driven using single-ended and differential signaling [11]. Modulation speed of 12.5 Gbps is possible with

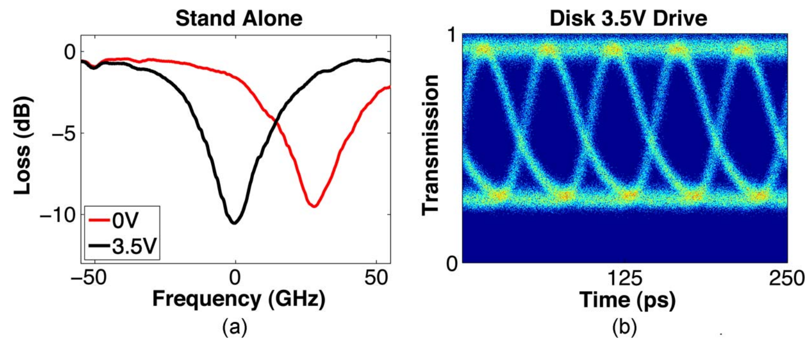

Fig. 2. Resonances and eye diagram of the discrete modulator. (a) The resonances show a Q of about 10^4 and a 30-GHz frequency shift with a 3.5-V applied reverse bias. If the carrier frequency is at zero detuning then the insertion loss is about 2 dB. (b) The discrete part 10-Gb/s eye diagram shows greater than 7 dB extinction.

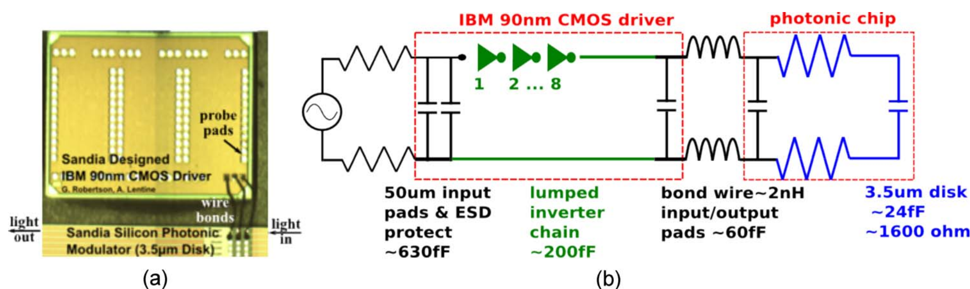

Fig. 3. Picture and circuit diagram of the 2-D integration. (a) The picture shows the IBM 90-nm CMOS driver chip (top) wire bonded to the silicon photonic chip (bottom). The integrated part is probed as indicated on the driver chip, and light is side coupled using lensed fibers. The on/off chip coupling loss is a total of about 20 dB. (b) The circuit diagram shows the capacitive contributions from pads, ESD protection, and the driver/modulator circuit.

BER $< 10^{-12}$ and its compatibility with high volume manufacturing has been thoroughly explored [21]. In this paper, we present the first demonstration of this device's performance when intimately integrated with electronics. However, this modulator should not be unique in its ease of monolithic integration with CMOS. Much of the work in silicon modulators uses the same or very similar substrates due to the requirements for single mode operation using a $\sim$1550-nm carrier wave. Therefore, work showing similar low voltage operation [10] and higher speeds [9] and extremely low voltage modulation in forward bias [12] should also be compatible.

The demonstration in [13] shows heterogeneous integration with a custom driver utilizing low energy.

3. Two-Dimensional Integration

In this paper, we demonstrate two concepts to integrate the photonic device. The first is by wire bonding a 90-nm technology node CMOS driver designed by our team and fabricated by IBM. Fig. 3(a) shows a picture of the integrated device. The IBM driver chip has probe pads and output pads that are then wire bonded to the photonic chip input pads. The photonic chip is diced exposing the waveguide end facets, which are tapered. Light is side coupled through the use of lensed fiber with an on/off chip insertion loss of 20 dB. Fig. 3(b) shows the equivalent circuit model of the integrated chips. The driver has eight stages and fans out from a 3X inverter to a 44X inverter, where the number in front of the X refers to the total gate width of the inverter transistors compared to the minimum size inverter. The inverter chain has combined capacitance of $\sim$200 fF. Also note the probe pad circuit elements shown in black. In addition to the pads themselves there is a

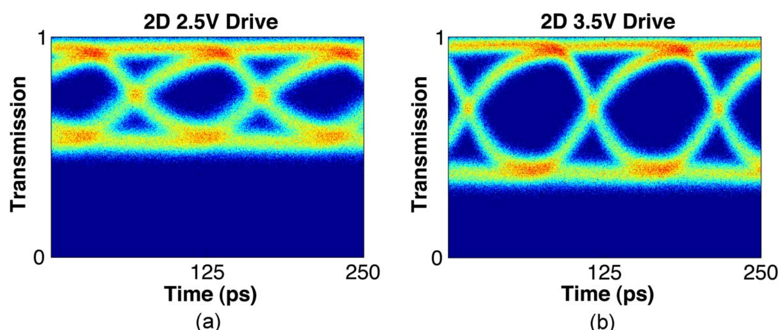

Fig. 4. The 5-Gb/s switching eye diagrams of the 2-D integrated electronics and photonics. The speed is limited by the driver circuitry. (a) The nominal drive voltage for the chip is 2.5 V, and at that amplitude, the extinction ration is about 3 dB. (b) The 3.5-V eye diagram shows 6-dB extinction.

parasitic capacitance from electrostatic discharge (ESD) protection diodes on the CMOS circuit, which alone contributes $\sim$600 fF.

The device was tested using an Agilent 8164B tunable laser source at a continuous wavelength of 1550 nm. Data was imprinted on this carrier by driving the inputs through a 50-Ω terminated probe with a $2^{31} - 1$ pseudorandom bit sequence (PRBS) from a Centellax bit error rate tester (BERT) at 5 Gbps. The BERT output was amplified from 1.5 V to 2.5 V and 3.5 V. Bit error rates were measured using the BERT attached to a 12-GHz bandwidth receiver. Two different driver (and V_{dd}) voltages were used which both yielded BER's $< 10^{-12}$. The eye diagram for the 2.5-V drive yields 3-dB extinction while the 3.5-V drive can generate a 7-dB extinction ratio. The driver was designed to run at 2.5 V; therefore, the 3.5-V data is the result of overdriving the part. The ESD protection at $\sim$600 fF coupled to the pad capacitance at $\sim$30 fF with a 50-Ω input limits the speed of the system to about 5 Gb/s above which, significant eye closure is seen. The electrical 3 dB BW of the driver chip is $\sim$10 GHz, but when coupled with the input capacitances of the ESD protected pads, this limits the operation of the integrated device to 5 Gb/s, as shown.

To calculate the energy per bit of this integrated modulator-driver the total power is calculated from the voltage and current and then divided by the bit rate. For the 2.5-V drive the current is 3.2 mA, for a total power consumption of 8 mW and energy per bit of 1.6 pJ/bit. In the case of the 3.5-V drive voltage, we find a drive current of 3.2 mA, total power consumption of 11.2 mW, and an energy consumption of 2.2 pJ/bit (see Fig. 4). These results are summarized and compared with the monolithic and discrete driver in the final section.

4. Monolithic Integration

The second demonstration is monolithic integration in the 0.35-μm CMOS process on which the discrete part has been manufactured. Fig. 5(a) shows a representational layout of the inverter stages and disk (not to scale). The driver consists of three inverter stages that are 2X, 6X, and 18X of the standard inverter size. The modulator signal line is connected to the final inverter stage. The process into which the modulator was integrated has five metal layers and uses 250 nm thick silicon for the active layers. This was convenient for integration because the standard optical design also uses 250-nm-thick silicon. The modulator and driver are connected at the metal 2 layer. Standard design rules for metal tiling were used above this layer to provide a consistent surface for planarization. An important difference in the processing of the integrated modulator is the use of a different dielectric cladding, which is discussed below.

Fig. 5(b) shows the equivalent circuit of the monolithic integration. This is essentially a simplified version of the 2-D integration. The pad capacitance in this case is not a significant contributor to the energy consumption. However, the larger gate length of the transistors used in a 0.35-m process limit the speed of the monolithically integrated device to 2 Gb/s.

For testing, the V_{dd} and ground are connected using DC probes. The V_{dd} for this device is 3.3 V. The IN, or gate, port is driven with 3.3-V amplitude signal using a high speed probe connected to the

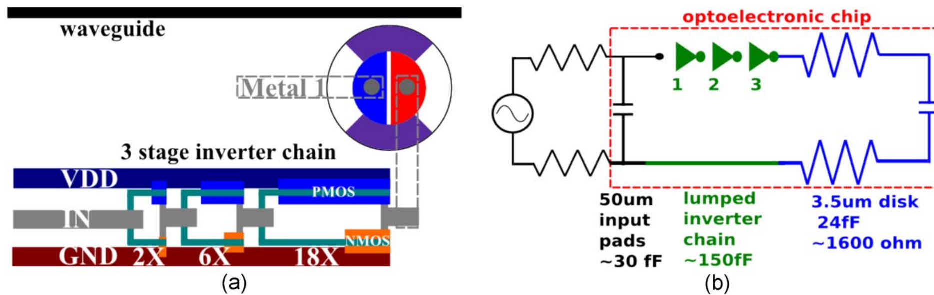

Fig. 5. Process layers and layout of the monolithic integration. (a) The layout (not to scale) consists of the 3.5-μm disk with waveguide and a three-stage driver. The driver stages are 2X, 6X, and 18X the standard inverter size. (b) The equivalent circuit of the monolithic optoelectronic driver and modulator chip is a simplified version of the 2-D integration. Not only is the contact pad capacitance for bonding eliminated, but the entire function fits within a few hundred micrometers.

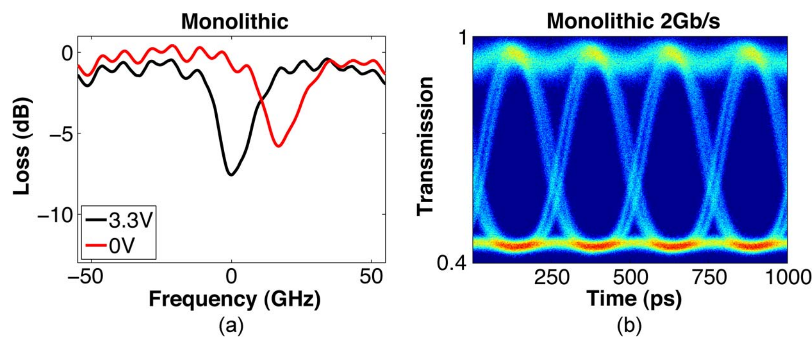

Fig. 6. DC and switching performance of the integrated part. (a) DC resonances are plotted and show that the extinction ratio has been degraded. One of the reasons for this is an air gap the oxide between the disk and waveguide. (b) The bandwidth is limited by the performance of the 0.35-μm technology used for fabrication. A clear eye with about 4-dB extinction is shown at 2 Gb/s.

Centellax BERT as described above. The probe was terminated with 50 Ω and the output of the BERT is amplified from 1.5 V to 3.3 V. In Fig. 6(a), we also plot the DC performance of this device (off chip coupling was again with lensed fibers and 20 dB of loss) because it shows that the extinction ratio is not as good as it is for the standalone device as was shown in Fig. 2(a). This is likely the result of different materials on the standard CMOS process being used on an optical modulator. The effect comes from a change in the deposited oxide over-cladding the device. Our process characterization indicates that the 350-nm gap creates a high enough aspect ratio that this oxide has difficulty filling. The result of the under filled high aspect ratio gap is an air hole or keyhole between the disk and the waveguide. This would cause higher index contrast between the disk or waveguide and gap material. This can reduce the coupling by leading to a smaller overlap integral [22] resulting in less extinction. However, better oxide filling can be obtained by engineering the oxide deposition process for photonics and electronics. While process development may be needed to optimize deposition and eliminate the keyhole, this is not a barrier for monolithic integration, but an opportunity to improve on this work. The Fabry–Perot fringes in this plot are the result of untapered waveguides at the diced facets. Tapering, as was done with the standalone device eliminates these.

Performance at 2 Gb/s with $< 10^{-12}$ BER is shown in Fig. 6(b). Here, the loss of extinction is evident as the performance is limited to about 4 dB. A new gap design, which takes into account the CMOS process steps that are marginally different from our standard optics process, should be able to restore the extinction. The CMOS driver has a 3 dB BW of $\sim$1.5 GHz.

The monolithic device running at a power supply voltage of 3.3 V draws 509 μA from the supply for power consumption of 1.68 mW, and at 2 Gb/s for a pseudorandom input, the energy per bit is 840 fJ/bit.

TABLE 1

Total energy consumption and bandwidth is summarized for each part, discrete, monolithic, and 2-D integrated. These calculations include the ESD protection

Device	Power	Energy	BW
Discrete Disk 3.5V	200uW	~50fJ/bit (w/o pads)	10Gbps
Monolithic 3.3V	1.68mW	840fJ/bit	2Gbps
2D 2.5V	8mW	1.6pJ/bit	5Gbps
2D 3.5V	11.2mW	2.2pJ/bit	5Gbps

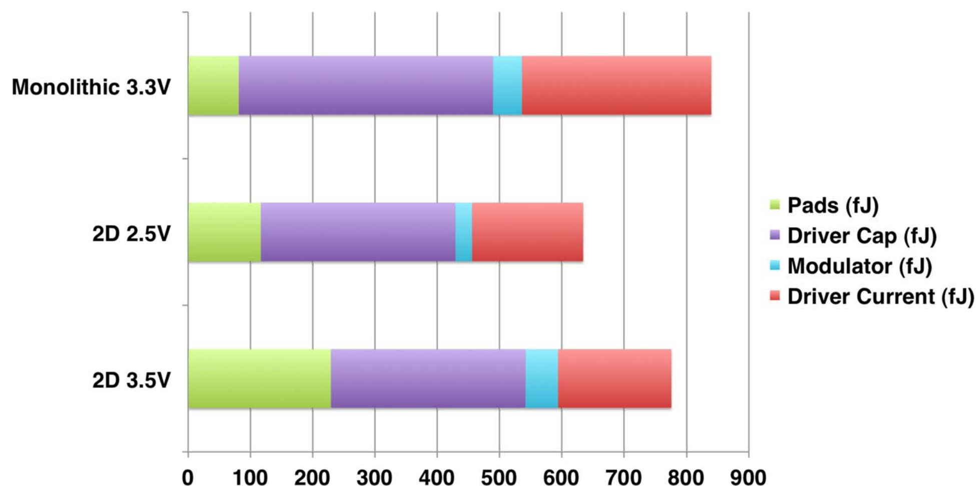

Fig. 7. Energy per bit consumed when the ESD protection is removed from the calculation. The smaller transistors in the 90-nm technology reduce both driver current and transistor capacitance making the two integrations comparable.

In testing monolithic devices, six chips were tested in total. Although the sample size is small, performance variation was not seen suggesting yield for this type of integration could be similar to typical silicon electronic yields. Previously studied resonator frequency variation is still evident in these devices and has been reported on [21].

5. Discussion

Table 1 gives a summary of the power and energy consumption of the discrete part and integrated parts from this demonstration. This table includes the effect of the ESD structures. The monolithic integration consumes less than ~840 fJ/bit, which is half of what the 2-D integration consumes, even though, in one case, the 2-D device is using less voltage. However, the greater energy consumption is almost exclusively due to the large ESD diodes in the 2-D device. This can be more easily identified in the detailed energy histogram analysis of Fig. 7, which pulls the ESD contribution out. Should the ESD diodes be eliminated, both integrations can achieve less than 1 pJ/bit. The optical modulator used in these integrations has been shown to consume energy as low as 3 fJ/bit and operate with a single volt or less [6]–[8], [11]. The current required for this level of switching is about 3 mA at its peak meaning much smaller drivers with a single stage could drive the devices. A single 3X inverter, for example in the 0.35-μm process we used, would add less than 20 fF, which at 1 V would result in total drive energies well below 50 fJ/bit.

We have demonstrated two possible integrations of a low-power silicon photonic modulator with CMOS electronics. The monolithic integration shows the ready integration that silicon photonics provides into standard CMOS manufacturing. Although our process is based on thicker silicon than

that typically used today on advanced processors, the application to a photonic transmitter chip with integrated drivers is apparent. The monolithic integration shows 840-fJ/bit modulation energy while the 2-D integration at similar voltages is comparable to that. However, these drivers provide much more current than is needed for the smallest modulators available today. With smaller drivers more compatible with the current needed to run a small modulator the energy per bit of monolithically integrated CMOS photonics and electronics can be pushed much lower.

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