Electronic Photonic Integrated Circuits for High Speed, High Resolution, Analog to Digital Conversion

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ABSTRACT

Progress in developing high speed ADC's occurs rather slowly - at a resolution increase of 1.8 bits per decade. This slow progress is mostly caused by the inherent jitter in electronic sampling - currently on the order of 250 femtoseconds in the most advanced CMOS circuitry. Advances in femtosecond lasers and laser stabilization have led to the development of sources of ultrafast optical pulse trains that show jitter on the level of a few femtoseconds over the time spans of typical sampling windows and can be made even smaller. The MIT-GHOST (GigaHertz High Resolution Optical Sampling Technology) Project funded under DARPA's Electronic Photonic Integrated Circuit (EPIC) Program is trying to harness the low noise properties of femtosecond laser sources to overcome the electronic bottleneck inherently present in pure electronic sampling systems. Within this program researchers from MIT Lincoln Laboratory and MIT Campus develop integrated optical components and optically enhanced electronic sampling circuits that enable the fabrication of an electronic-photonic A/D converter chip that surpasses currently available technology in speed and resolution and opens up a technology development roadmap for ADC's. This talk will give an overview on the planned activities within this program and the current status on some key devices such as wavelength-tunable filter banks, high-speed modulators, Ge photodetectors, miniature femtosecond-pulse lasers and advanced sampling techniques that are compatible with standard CMOS processing.

Keywords: Electronic photonic integrated circuits, silicon photonics, high index contrast, optical sampling, optical analog-to-digital conversion, integrated femtosecond lasers

1. INTRODUCTION

Rapid progress in CMOS technology combined with advances in parallel computing architectures has made Teraflop digital processors a reality. However, the wealth of new system capabilities offered by such processors cannot be fully exploited due to the limited performance of ADC's. ADC performance at high sampling rates is fundamentally limited by the timing jitter of the electronic clocking circuits, typically a quarter of a picosecond or higher. However, optical clock pulses from a mode-locked laser (MLL) exhibit sub-10 femtosecond timing jitter; thus using photonic sampling has the potential for order-of-magnitude improvement in ADC performance.

Photonic analog-to-digital conversion techniques have been the subject of extensive research in recent years [1,2,3]. Photonic ADC architectures provide significant improvements over electronic ADC due to reduced clock jitter and the ability to channelize the sampled data for electronic quantization at lower data rates. There are two standard architectures for photonic ADC systems. The first, known as photonic time stretch, utilizes dispersion of a chirped optical pulse to temporally magnify a segment of a wideband signal to be sampled [3]. After magnification, the signal can be electronically sampled and quantized at a lower sample rate. Photonic time stretch systems suffer due to dispersion-induced attenuation of high-frequency components in the analog waveform. This distortion may be reduced

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using single sideband modulation [4,5], but this approach complicates the system architecture. A second photonic ADC architecture is known as time-interleaved optical sampling. With this approach, a stream of pulses, or a single chirped pulse, is used to sample the analog signal at a high sample rate. After sampling, the pulses are separated into several lower-rate streams using time-division multiplexing (TDM) [6] or wavelength-division multiplexing (WDM) [7] techniques. The TDM approach simplifies the requirements on the optical sampling source. However, the TDM demultiplexer can be difficult to implement and may limit the maximum sample rate to a few GSa/s. With the WDM approach the multiwavelength stream of optical pulses is de-interleaved using passive WDM demultiplexers. As with the photonic time stretch ADC, the number of parallel electronic ADCs required to implement continuous-time sampling with the time-interleaved optical sampling ADC makes the implementation of such a system challenging. The highest reported continuous sample rate for a time-interleaved photonic sampling ADC is 12 GSa/s in a system consisting of three parallel electronic ADCs operating at 4 GSa/s.

2. OPTOELECTRONIC ADC-CHIP

In the scheme discussed here, see Figure 1, we channelize the optical clock in time using precisely-tuned WDM filters to create time-interleaved optical sampling signals, each operating at the rate of the optical clock. The total sampling rate is then the optical clock rate times the number of WDM channels. There are other time-interleaved or time-

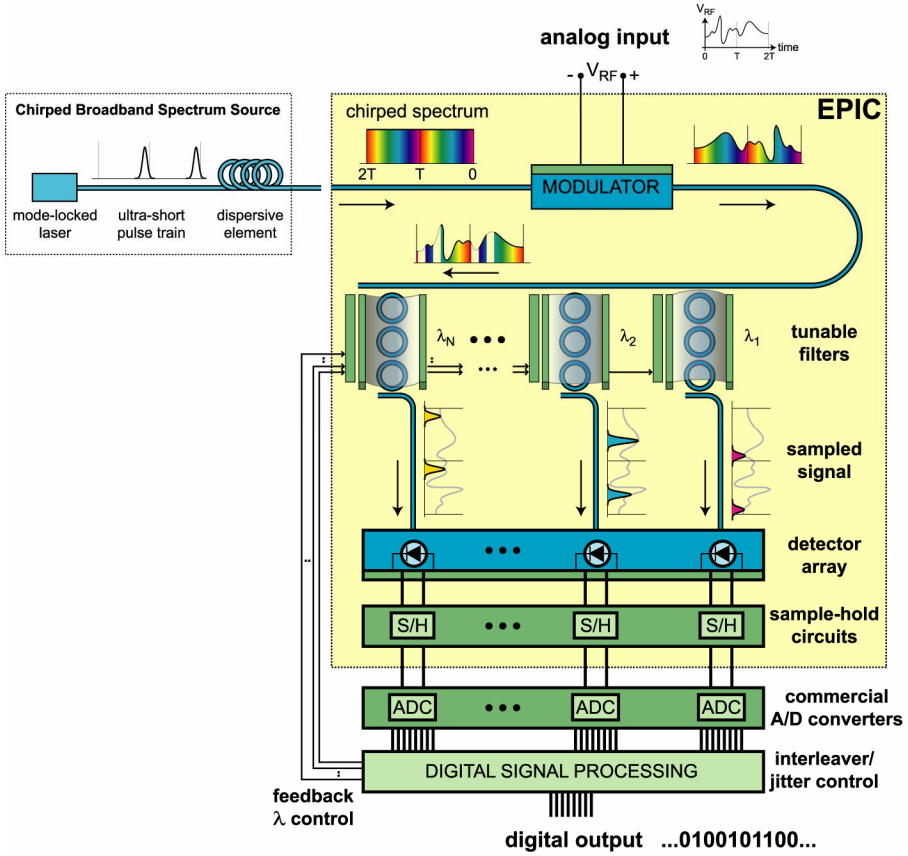


Figure 1: High-speed, high resolution optical sampling chip. A low-jitter femtosecond laser with repetition rates of a few hundred MHz or a few GHz emitts a stream of pulses that is dispersed. Dispersion is chosen such that the chirped pulses cover the time interval between the pulses. The RF-waveform to be sampled is imprinted on the chirped pulse stream via an electro-optic modulator. The optical output is channelized via a WDM-filter bank with precisely-tuned center frequencies that map to certain sampling times. The signals from each channel, which correspond to time interleaved sample sequences can be separately digitized in low rate high resolution ADC's, which might benefit from an on-chip Ge detector array and optically enhanced sample and hold-circuits.

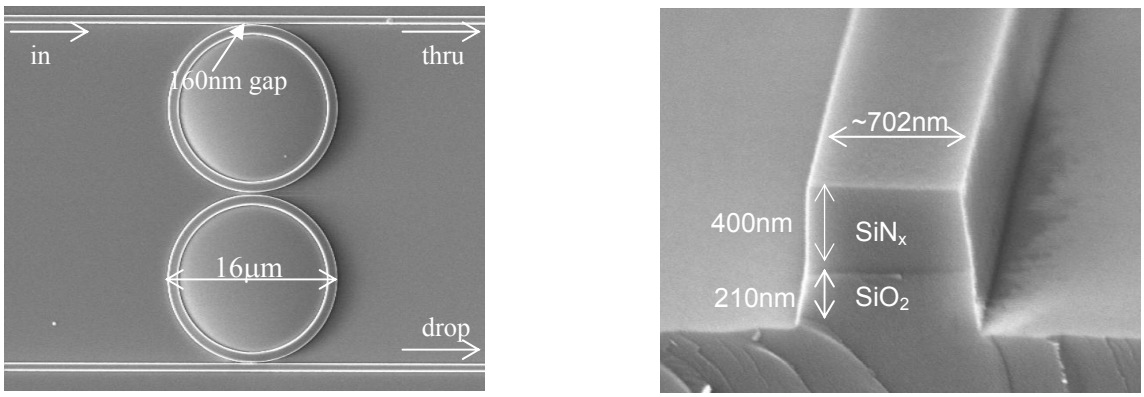
stretched techniques for achieving high sampling rates through time segmentation, each with its own advantages/disadvantages. Channelization using passive WDM components represents another powerful feature of optical sampling. However, in order to realize the high resolution, the sampling times of the interleaved channels must be uniform, the converter gains from each channel must be closely matched, and the sample memory effects must be minimal [8]. These characteristics require monitoring and very tight feedback control of the WDM filters.

The applications we are targeting—all-digital radar, for example—require very high density of integration. Thus all of the above functionalities should be integrated on a single chip: optical sampling, WDM filters, feedback control. The technological roadmap requires the development of a number of devices: low-loss waveguides in high-index-contrast materials (HIC) supports higher densities of photonic components and larger free spectral range (FSR) optical resonators); WDM filters that can be tuned dynamically; wideband optical modulators, Ge- photodetectors, femtosecond lasers and novel optically controlled sampling techniques. All these devices and techniques must be integrated on a CMOS compatible technology platform. In the following we discuss progress made towards the key components for this optoelectronic sampling technology

3. HIGH INDEX CONTRAST FILTER BANK

Microring resonators were first proposed as integrated optical wavelength filters by Marcatili in 1969 [9]. Applications that envision complex EPIC functionality such as the proposed ADC chip call for dense optical integration, and require microrings with *low loss*, a *large free spectral range* (FSR), and a drive to *wavelength-scale resonator sizes*. The latter two of these three key requirements invariably call for implementation in high-index contrast (HIC), which has presented many challenges since HIC microrings were first investigated [10,11,12,13]. As a further complexity the proposed ADC chip requires the ability to accurately control the resonant frequency of each microring and reduce crosstalk between the individual filters in the WDM filter bank.

The microring resonator filter design used for fabrication of the WDM filter banks for the proposed ADC converter is very similar to the design discussed in [14]. By utilizing this design with the HIC materials of silicon-rich silicon nitride (n =2.2 @ 1550 nm) and silicon dioxide (n =1.455 @ 1550nm) a very wide FSR of 20 nm in realized. Also the HIC allows for a bending radius as small as 8 μm enabling the possibility for the creation of very densely integrated photonic systems. The filter design was optimized to achieve the objective of a 3 dB bandwidth of 50 GHz and less than 30 dB crosstalk for 150 GHZ spaced channels. These parameters resulted in a design where the critical feature size of the gap between the bus and ring waveguides is 160 nm (Figure 2a).



(a) (b)

Figure 2: (a) Top view of second order microring resonator filter. (b) Cross-section view of bus waveguide showing smooth vertical sidewalls.

In order to fabricate microring resonator filters to meet the design requirements, direct write scanning electron beam lithography (SEBL) was used due to its combination of high resolution and high level of dimensional control. The basic fabrication process used is similar to that described in [15]. The silicon wafer was initially iodized to grow a 3 μm-thick

undercladding layer of SiO_2 to prevent power leakage to the substrate. Next, a 400 nm layer of silicon-rich silicon nitride (SiN_x) was deposited by low pressure chemical vapor deposition (LPCVD) to serve as the high index core material. A Raith 150 SEBL system was used at 30 keV to write the pattern into a 200 nm resist layer of poly-methyl-methacrylate (PMMA). A layer of Aquasave, a conducting polymer manufactured by Mitsubishi Rayon, was spun on top of the PMMA in order to prevent charging from the electron beam. After developing the PMMA, Ni was evaporated on to the device and a lift-off process was used to make a hardmask. The waveguides and filters were created by reactive ion etching (RIE) the sample with a mixture of CHF_3 and O_2 gases to etch through the 400 nm layer of SiN_x. The etch gas was then switched to CHF_3 only in order to etch 200 nm into the SiO_2 undercladding layer. Both of the RIE etch recipes were optimized to produce smooth, vertical sidewalls in each material as shown in figure 2. Due to the lack of an etch stop the actual fabricated device had a slight over etch of 10 nm, which was within design tolerances.

Controlling the resonant frequency of HIC microring resonator filters requires an extremely high level of dimensional control. The resonant frequency of a microring resonator is determined by Equation 1, where m is an integer, λ is the resonant wavelength, R is the ring radius and n_{eff} is the effective index of refraction of the ring waveguide. It turns out that both R and n_{eff} can be controlled with lithography. R is simply controlled by changing the radius of the ring in the design layout whereas n_{eff} can be controlled by changing the width of the ring waveguide. For the design used the resonant frequency shifts 30 GHz for every nanometer increase in average ring waveguide width. A major problem that is encountered with changing these parameters in the design layout is that one is limited to discrete steps due to the pixel size used by the SEBL system. For the writing technique used, the discrete step sizes are limited to 6 nm and 12 nm for the ring radius and ring waveguide width respectively. This results in discrete frequency shifts of 104 GHz steps when changing the radius and 360 GHz shifts when changing the ring waveguide width. This means in order to achieve

$$m \cdot \lambda = n_{eff} \cdot 2\pi \cdot R \tag{1}$$

our objective of 150 GHz channel spacing a different technique needs to be used to control the resonant frequency that is not limited by the pixel size of the SEBL system. The technique used is dose modulation, an extension of the concept of dose compensation, which has previously been used to correct for proximity effects and coupling induced frequency shifts in microring resonators as explained in [16]. Dose modulation is the practice of slightly changing the electron dose that the rings are written with allowing for the average ring bus width to be changed on the tens of picometer scale. The frequency shift induced by dose modulation is dependent on many factors including the waveguide design, resist, base dose, and developer. Thus dose modulation needs to be very preciously calibrated for both the design and the fabrication process to be used. Calibration was done by fabricating a series of devices that were comprised of a waveguide coupled to two microring resonator filters. One of the microring filters serves as a reference point while dose modulation is used on the test microring filter. This is done for different magnitudes of dose modulation and by comparing the relative frequency shifts the frequency dependence on dose can be calculated. From the calibration it is found that the frequency shift is linearly dependent on dose modulation, shifting -18 GHz for each percent of the base dose increased, for increases less than 8% of the base dose. It was also found during calibration that to a first approximation frequency shifts due to dose modulation and radius changes can be assumed to add linearly. This technique allows us to overcome the limitation of discrete frequency shifts permitting the fabrication of any desired channel spacing. This technique combined with changing the radius was used to make 8-channel second order filter banks with channel spacing of 90, 104, 120, 140, 145, 150, 155, 160, and 180 GHz to demonstrate our ability for fabricating filter banks with precisely controlled channel spacings.

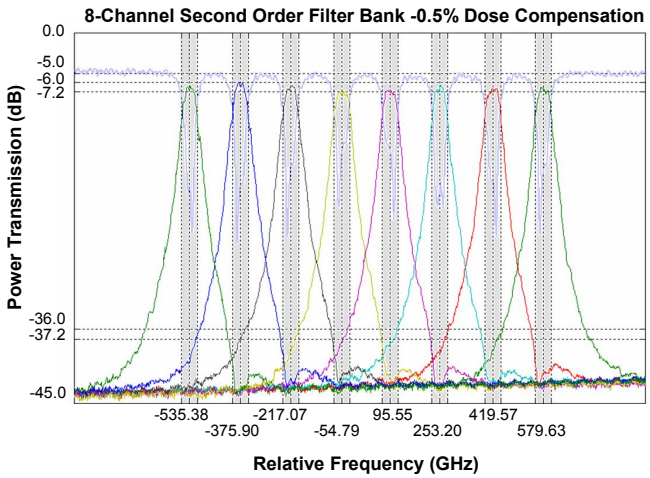


Figure 3: Through- and drop-port characteristics of filter bank with second order single stage filters and 159 GHz channel spacing. Frequencies are all relative to 1540 nm.

Optical transmission measurements were performed on the fabricated filter banks using a tunable

laser in a fiber to fiber optical characterization set up. Figure 3 shows the measured transmission response for the filter bank fabricated with a target bandwidth of 50 GHz and channel spacing of 150 GHz. The actual filter bank response had a bandwidth of 46.5 GHz and an average channel spacing of 159 GHz with a standard deviation of 5 GHz. This offset in channel spacing is due to a 4.2% higher frequency dependence on radius changes than expected, since it is evident in all of the filter banks with different channel spacing. This error can be greatly reduced in future fabrication runs through careful calibration experiments similar to the ones preformed for dose modulation. The standard deviation is due to stochastic variations that can not be eliminated due to their random nature. It is likely that this number will be lower in future fabrications since the tip for the SEBL system had been recently replaced and the electron beam current had not completely stabilized by the time of fabrication. Overcladding and heater designs are being investigated so that thermal trimming can be used to make slight adjustments to the resonant frequency of the microring resonator filter to correct for small errors due to calibration errors and stochastic variations. The drop loss of the filters, averaged over 40 filters to reduce errors from coupling variations, is calculated to be 1.5±0.5 dB. Simulations indicate that this drop loss can be accounted for by a propagation loss of approximately 8 dB/cm. Loss measurements performed on ridge waveguides fabricated in SiN_x showed that it has an intrinsic absorption loss of 7.5±2 dB/cm at 1540 nm. Therefore, the scattering loss due to sidewall roughness in our fabricated devices is maximum on the order of 1dB/cm.

One important consideration when designing microring resonator filters for filter banks is the adjacent channel crosstalk. For the proposed ADC as well as many other applications it is important to minimize the adjacent channel crosstalk. The filters fabricated give -30 dB crosstalk for 150 GHz channel spacing as predicted from the design. For the designed microring resonator filters the crosstalk will remain at –30 dB as the bandwidth and channel spacing are scaled down proportionally. A common way to decrease the adjacent channel crosstalk is to use higher order filters. The problem with higher order filters is that they are much more sensitive to small defects. A better way to improve the adjacent channel crosstalk is to use a multistage filter design since it is much less sensitive to small defects than higher order filters as described in [14]. In a two stage filter layout both the thru and drop signals go through two sets of second order filters. Figure 4 shows the thru and drop response measured for a two stage second order filter fabricated with the same basic filter design used for the filter banks. As seen in the figure, by multistaging the filters it is possible to greatly decrease the adjacent channel crosstalk without changing the filter design. The crosstalk is measured to be over 40 dB down but cannot be accurately determined since it is below the noise floor of the measurement system used. Simulations show that the two-stage filter should have -50 dB crosstalk as desired for the proposed ADC. The only major disadvantage with using the two stage design is that the overall drop loss is increased since the drop signal must now pass through two filters.

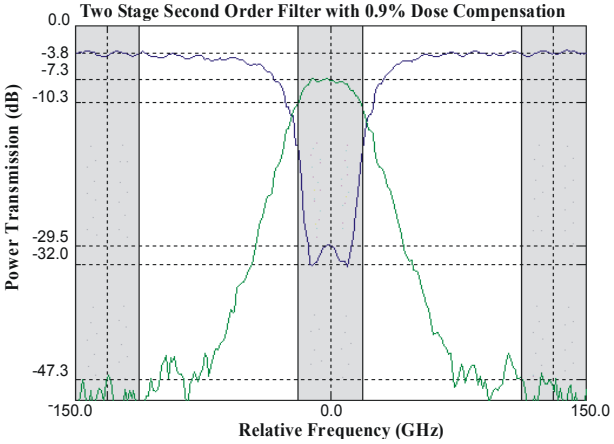


Figure 4: Thru and drop response of a two stage second order microring resonator filter with a bandwidth to channel ratio of 1:3.

Overall the design and fabrication of microring resonator filter banks used for the proposed ADC-EPIC chip shows great promise. By small modifications in the filter design the bandwidth can be decreased allowing for scaling of the channel spacing to keep the desired 1:3 bandwidth to channel spacing ratio. Also, through the combination of changing the ring radius and using dose modulation it has been shown that the resonant frequency of the filters can be precisely controlled to meet any desired target channel spacing. In future fabricated microring resonator filter banks, heaters will be used to thermally correct for small frequency spacing errors due to calibration errors and stochastic variations. Also by using multistage filters it will be possible to decrease the adjacent channel crosstalk to -50 dB without having to switch to more complex and sensitive higher order filters.

4. HIGH SPEED SILICON MODULATOR

One of the most important electro-optic devices for future electronic-photonic integrated circuits, and for the envisioned ADC-Chip in particular, is a silicon-based high-speed electro-optic modulator that converts electronic signals into the

optical domain. Plasma and thermal effects in silicon have long been known as an efficient means to achieve such modulation [17]. Early on, p^+in^+-structures based on the plasma effect have been proposed and realized for silicon-based electro-optic phase and amplitude modulators with switching speeds up to 10 MHz [17,18]. The response speed of these devices is limited by carrier recombination. Very recently a modulator based on a MOS structure has been reported operating at frequencies up to 10 GHz [19]. However, this device needs an applied voltage of 5~10 V. The key figure of merit (FOM) for a phase-modulator is the product between the applied voltage to reach a π-phase shift, V_π, and the length of the device, L. The above device had an FOM greater than 10 Vmm. Here, we further improve a design for a high-speed electro-optic modulator based on HIC silicon buried waveguides with minimum optical loss and FOM as necessary for an ADC-Chip [20].

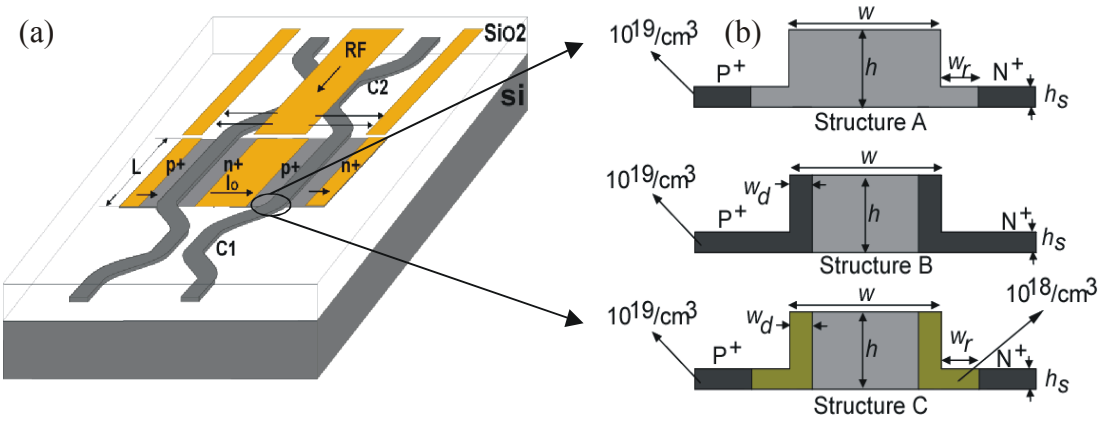


Figure 5: (a) Mach-Zehnder modulator with forward biased p^+in^+-phase modulator sections. (b) Different possible doping profiles for the Si buried waveguides used for the modulators.

A schematic layout of the proposed modulator is shown in Figure 5. Figure 5(a) shows a conventional Mach-Zehnder arrangement, and Figure 1(b) shows the most important sub-component of the modulator, the electrically driven phase modulator section. The contact resistivity is assumed to be small, about 10^{-7} Ωcm^2 [21]. Therefore, most of the voltage drop is across the i-region of the p^+in^+-modulator. For short carrier lifetimes, that can be controlled to the order of picosecond using doping or ion implantation [22], the electric field can be increased to a level where the carriers almost drift at the silicon saturation velocity, v =10^7 cm/s. The high velocity of the carriers increases the modulator bandwidth, $f_{3dB}=2.2/(2\pi\tau)$, where $\tau = w/v$ and w is the length of the i-region. The modulation speed can also be increased by decreasing w.

As shown in Figure 5(b), three kinds of p^+in^+-diode structures are investigated to achieve optimum modulator performance. The modulation bandwidth is increased by moving the highly doped P^+/N^+ regions in the waveguide as close as possible to the optical mode by decreasing the length of the undoped region w_r in structure A, or even moving the higher doped regions inside the buried waveguide as in structure B. However, structure B then leads to high optical losses of over 60 dB/cm due to the proximity of high doping to the optical mode. Much lower loss is achieved with structure C where the sidewalls of the waveguide are only weakly doped and higher doping is only applied to those sections of the waveguide that are not touched by the optical field. The sidewall doping also greatly improves equalization of the carrier distribution across the intrinsic i-region and therefore decreases the FOM of the modulator. Figures 6-8 show the simulated performance of these structures A and C. The optical loss, shown in Figure 6(a), of structure A as a function of height h_s and with different w_r for the current leads is around 0-20 dB/cm due to the doping and 3-35 dB/cm including free carrier absorption induced by the 3V DC forward bias. As shown in Figure 8(a), the optical loss of structure C is only slightly larger than for structure A. Thus, the higher sidewall doping in structure C does not add much additional optical loss. However, the 3 dB corner frequencies of 29-35 GHz for structure C (w_d = 50 nm) are about 20% larger than structure A and C (w_d=0nm) (see Figure 8(b)). The short intrinsic width in structure C (w_d = 50 nm) plays an important role in enhancing the modulation bandwidth. Finally, the FOM of structure A is larger than structure C, around 3-12 Vmm as shown in Figure 6(b). A comparison of Figure 7(b) and 8(b) shows that structure C (w_d = 0 nm) has about 4% higher FOM than structure C (w_d = 50 nm), because the sidewall doping reduces the area where the carrier density can be changed by the current flow. Therefore, structure C (w_d = 0 nm) has the smallest FOM and structure C (w_d = 50 nm) shows the largest modulation bandwidth.

Based on the discussion above, structure C was chosen for a full high-speed modulator design. In the following we use dimensions h_s = 50 nm, w_d = 50 nm, w_r = 200 nm, w = 450 nm, and h = 250nm. The high and low doping levels are 10^{19}/cm^3 and 10^{18}/cm^3, respectively.

Detailed two-dimensional simulations have been carried out for a device implementing structure C. The static I-V characteristics of the phase modulator section in terms of the average current density flowing through the intrinsic zone

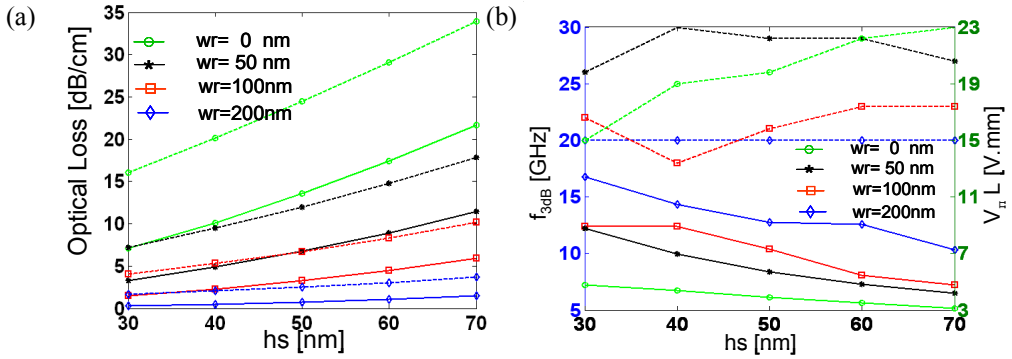


Figure 6: (a) Optical loss of structure A due to doping (−) and with additional carrier injection (--) (b) f_{3dB} (--) and $V_\pi L$ (−) of structure C (w_d = 0 nm), τ = 10 ps, V_{DC} = 2.5V

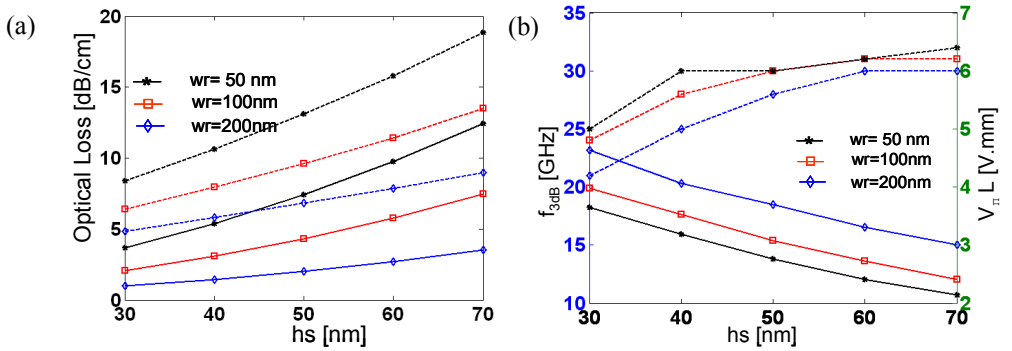


Figure 7: (a) Optical loss of structure C (wd = 0 nm) due to doping (−) and with additional carrier injection (--) (b) f_{3dB} (--) and $V_\pi L$ (−) of structure C (wd = 0 nm), τ = 10 ps, V_{DC} = 2.5V

as a function of applied voltage is shown in Figure 9(a) for three different intrinsic region carrier lifetimes. For voltages greater than 5V the current strongly saturates. The AC characteristics of the device are determined by computing the small signal modulation transfer function between effective index change in the phase modulator section and the applied

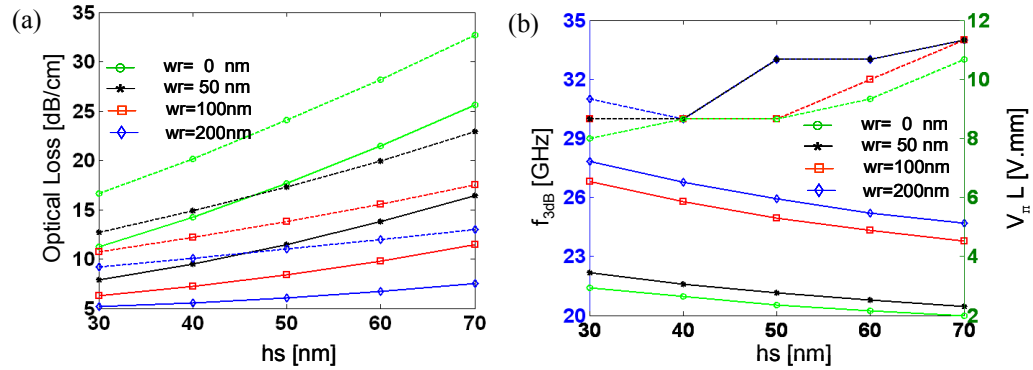


Figure 8: (a) Optical loss of structure C (wd = 50 nm) (−) due to doping and with additional carrier injection (--) (b) f_{3dB} (--) and $V_\pi L$ (−) of structure C (wd = 50 nm), τ = 10 ps, V_{DC} = 2.5V

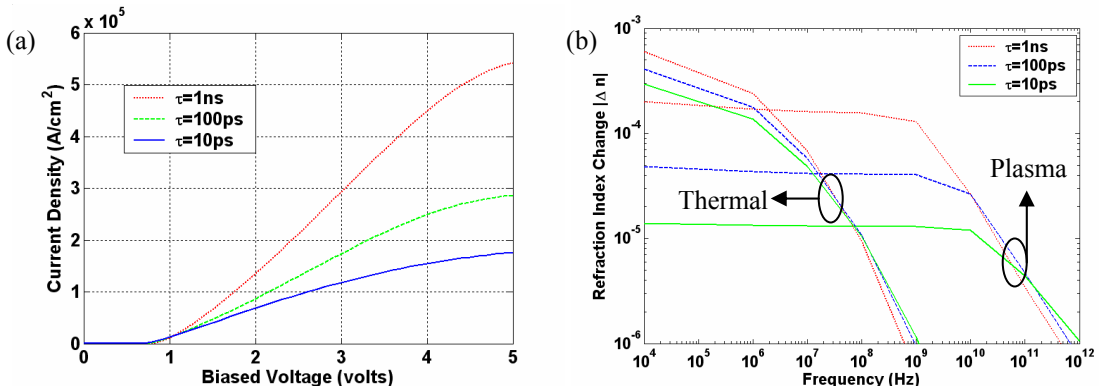


Figure 9. (a) Modulator I-V-characteristics; (b) Effective index change due to plasma and thermal effects for τ = 10 ps (solid), 100ps (dashed), 1ns (dotted) in structure C (w = 450 nm, h = 250 nm, h_s = 50 nm, w_r = 200 nm, w_d = 50nm)

voltage. The modulation speed of a pin-diode depends critically on both the carrier recombination time and drift velocity, i.e. how fast carriers can be removed from the intrinsic zone. Figure 9(b) shows the amplitude of the effective index change due to both thermal and plasma dispersion effects for an assumed sinusoidal drive voltage modulation with amplitude of 0.1V. For a structure with a carrier lifetime equal to or shorter than 1ns, the 3dB corner frequencies due to recombination are $f_{3dB} = 1/4\pi\tau$ = 8 GHz, 0.8 GHz, 0.08 GHz for τ = 10 ps, 100 ps, and 1 ns, respectively [19]. The simulations gave f_{3dB} = 32 GHz, 15 GHz, and 1.5 GHz, as shown in Fig. 9(b). This high modulation bandwidth is enabled by the almost saturated drift velocity of the electrons. For frequencies greater than 100 MHz, the plasma effect dominates the thermal effect. At frequencies below 100 MHz, thermal effects dominate because the thermal time constant is about 300 ns and, therefore, much longer than the carrier lifetimes used in the simulations. This is of major importance, because both effects have opposite signs and therefore there exists a frequency range between 1-100 MHz where the response is zero. For this design, a 6 mm length is necessary for a π phase shift at a 1 Volt bias because $V_\pi L$ is equal to 6 Vmm as indicated in Figure 8(b). The DC-power and the dissipated microwave power of a 6 mm long section are P_{DC} =3.6 W and P_{AC} =500 mW, which are not excessive.

This analysis shows that a high-speed electronic carrier-injection modulator based on a HIC buried Si-waveguides and forward biased integrated PIN-diode sections with operating frequencies as large 32GHz can be reached while maintaining a low insertion loss of only 3dB and a low figure of merit of 6 Vmm. The fabrication of this modulator structure is in progress at MIT Lincoln Laboratory.

5. GE PHOTODETECTORS

Strained germanium films have the required responsivity and speed to serve as photodetectors up to the 1.55 μm wavelength range. Thus, integrating Ge films onto silicon (Ge/Si) substrates into a CMOS-compatible process is an attractive goal for making arrays of on-chip detectors that can be used in an electronic-photonic ADC-chip. In this work, Ge films are deposited by Low Pressure Chemical Vapor Deposition (LPCVD) in an Applied Materials Epitaxial Reactor and the optical and electrical properties of Ge photodiodes is examined.

It has been demonstrated in Ultra High Vacuum Chemical Vapor Deposition (UHVCVD) systems that depositing a low temperature Ge layer (seed layer), followed by the deposition of a high temperature layer (cap layer) with subsequent annealing, can create a smooth, planar Ge film on a (100) silicon substrate with threading dislocation density on the order of 10^7 cm^{-2} [23]. This two-step deposition process has been successfully adapted to an LPCVD system. The seed layer is grown at 335°C, 30 Torr, and the cap layer is grown at 700°C, 30 Torr. After annealing at 900°C for 30 minutes, the blanket Ge films have threading dislocation densities of ~2 x 10^7 cm^{-2}. These Ge films experience a slight tensile strain after removal from the deposition chamber due to the mismatch between the thermal expansion and contraction coefficients for the germanium film and underlying silicon substrate. This tensile strain lowers the direct bandgap for the Ge film from 0.8eV to 0.78eV, giving these Ge films high absorption coefficients for wavelengths up to 1.6 μm [24].

Approximately 2 µm-thick intrinsic Ge films were deposited on p+ (100) Si substrates, and capped with a 0.2 µm N+ polysilicon layer to create a vertical *pin*-photodiode (Figure 10 inset). The IV characteristics of the photodiodes fabricated with the blanket Ge films are shown in Figure 10. The reverse leakage current at 300K and a – 1 volt bias is ~40 mA/cm^2, with the reverse leakage current of the diodes being perimeter dominated for diodes less than 1 mm^2 in surface area. The perimeter dominated reverse leakage current is believed to be due to surface states introduced during the Ge passivation process. This hypothesis is supported by the voltage and temperature dependence of the reverse leakage current. The responsivity as a function of wavelength for a 100 µm x 100 µm diode without AR-coating and a

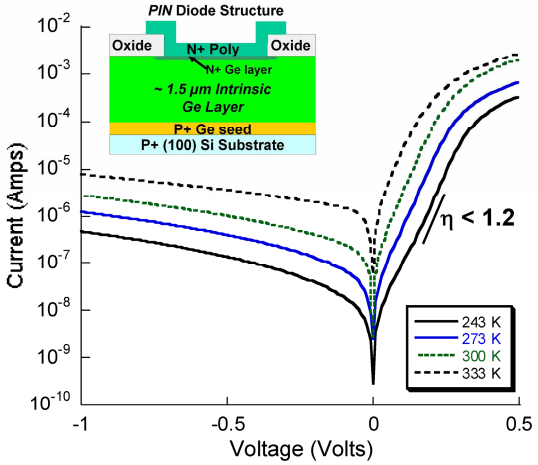


Figure 10: IV characteristics of a 100x100 µm diode as a function of temperature. The diode has an ideality factor less than 1.2 at 300K with a perimeter dominated reverse leakage current of ~55 mA/cm^2 at –1 volt bias. Inset shows a schematic of a diode cross-section.

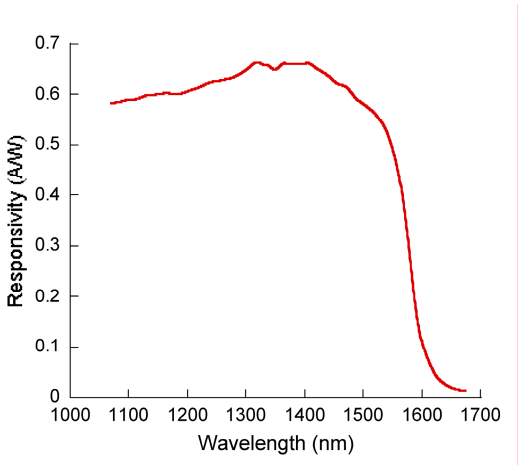


Figure 11: Responsivity versus wavelength for a 100x100µm diode with no AR-coating. The diode has a reverse leakage current of 32 mA/cm^2 at –1 volt bias and a responsivity of 0.5 A/W at a 1.55 µm. Below 1.2 µm the responsivity drops off due to absorption in the underlying silicon substrate.

reverse leakage current of 32 mA/cm^2 at –1 volt bias is shown in Figure 11. At a 1.55 µm wavelength, the Ge film has a responsivity of 0.5 A/W. Below 1.2 µm, the p+ silicon substrate begins to strongly absorb the incoming light as shown by the drop in responsivity. The frequency response of a 20 µm x 100 µm photodiode to a 1 picosecond pulse of light at a wavelength of 1.04 µm is shown in the inset of Figure 12. At a –5 volt bias, the diode is measured to have a 3dB frequency of 1.4 GHz. The inset shows the 100 ps rise time of the photodiode which is 7 times faster than the fall time of 700 ps. The lack of symmetry in the rise and fall may be associated with interfacial trap states at the N$^+$-polysilicon, dielectric, and Ge boundaries. This long fall time is believed to be a limiting factor in the frequency response of the photodiodes.

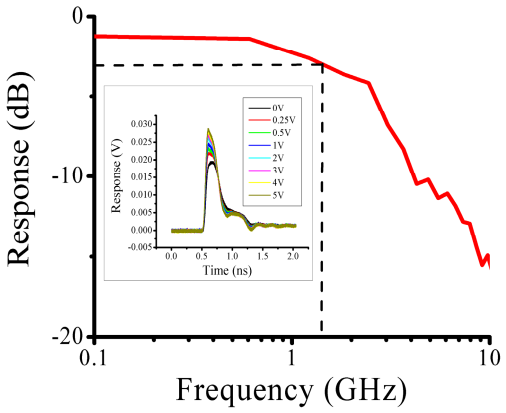


Figure 12: Fast Fourier transform of the photoresponse of a –5 volt biased 20x100 µm diode to a 1 picosecond laser pulse at a wavelength of 1.04 µm. Inset shows the photoresponse at various biases. The long fall time of the photoresponse is believed to limit the diode frequency response.

The photodiodes are required to translate pulse amplitude information into an electrical signal with sufficient linearity to achieve the proposed high ENOBs for the ADC system. To characterize the linearity, we measured the spur-free dynamic range (SFDR) of the diodes using the test setup shown in Figure 13(a). To calculate the SFDR, the spectrum of the photodiode response to a two-tone RF-modulated input is measured as a function of modulation amplitude. As shown in the microwave spectrum analyzer screen inset to Figure 13(a), third-order nonlinearities produce in-band intermodulation distortion products (IMD3) that limit the dynamic range of the detector.

To ensure that observed nonlinearities are caused by the diodes, the output of the link laser was examined by using a lightwave front-end to the microwave spectrum analyzer and by replacing the Ge photodiodes with industry-standard Epitaxx InGaAs p-i-n photodiodes designed for CATV applications. To complete the data required to calculate SFDR, the noise floor of the link was measured, roughly integrating over a 2-GHz bandwidth with the microwave spectrum analyzer. This data and the calculated SFDR are shown in Figure 13(b). The demonstrated 34-dB SFDR of this link would currently allow for 5.6 effective bits if it was the limiting factor in the system's performance.

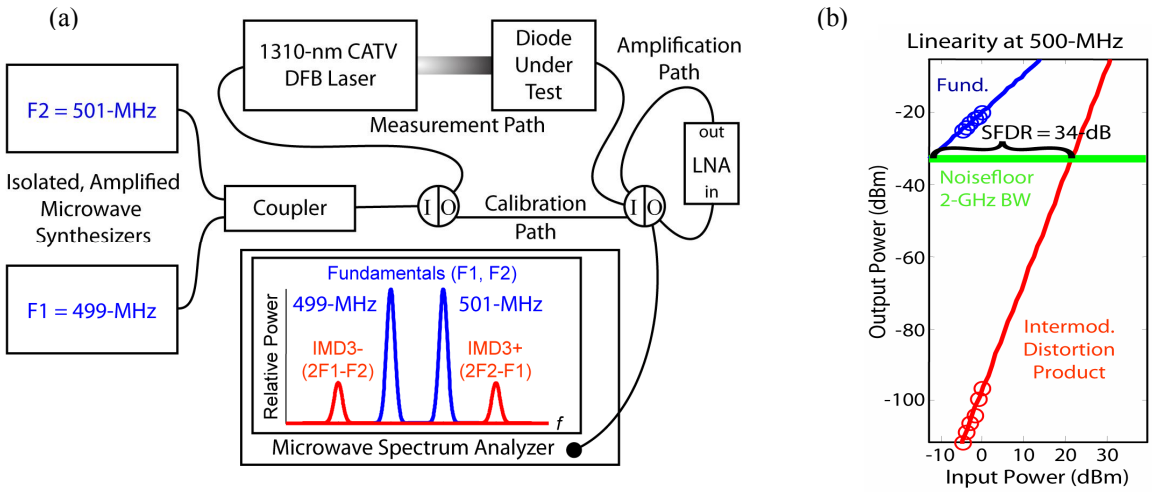


Figure 13: (a) Diagram showing the SFDR measurement setup. The I/0 blocks are microwave switches that enable switching between the measurement path and the calibration path, as well as the insertion of the optional amplification path. The block labeled LNA in the amplification path is a low-noise amplifier. (b) Spur-free dynamic range measurement on a 100x100μm Ge photodiode. The diode was biased at -3V

In summary, photodiodes with ~40 mA/cm^2 reverse leakage currents at 300K and –1 volt bias greater than 0.5 A/W responsivity and a 34 dB SFDR for a 2-GHz noise bandwidth have been fabricated. These diodes also have 3 dB frequencies in the GHz range, and it is believed that improved passivation of the Ge films will further improve the frequency response and the reverse leakage current of these CMOS compatible Ge photodetectors.

6. OPTICALLY ENHANCED SAMPLING

Recently, various architectures utilizing low-jitter optical sampling of wideband signals in high-speed data conversion have been studied and implemented [1,25,26]. But unlike earlier work, this project investigates the use of optical components to perform low-jitter *sub*-sampling of narrowband signals (e.g., 1-10 MHz BW) centered at high frequency RF carriers (e.g. 40 GHz).

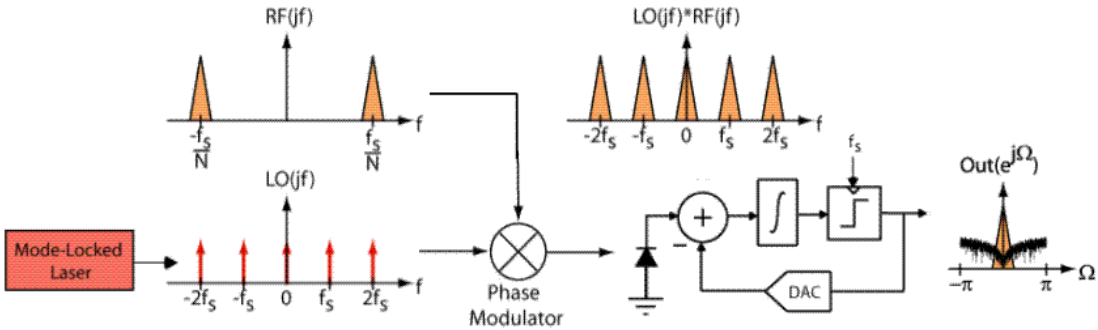


Figure 14: System diagram, comprising mode-locked laser, phase modulator, and continuous-time ΔΣ

The proposed architecture is shown in Figure 14, and comprises a mode-locked laser, a resonant optical phase modulator, and an optical-electrical ΔΣ ADC. Here, the low-jitter laser is leveraged to perform sub-sampling of an RF signal, aliasing replicas of the RF-signal at every harmonic of the pulse train. Immediately following the modulator is an optical-electrical continuous-time ΔΣ ADC, that leverages oversampling and noise shaping to achieve high precision digitization of the narrowband signal.

Prior work employing electronic sub-sampling architectures suffered lower SNR than other conversion techniques due to noise-folding from aliasing, and noise skirts arising from local oscillator aperture jitter [27,28,29] (See Figure 15). Noise-folding can be minimized through band-pass filtering of the RF prior to mixing, as was done in the previous work. However, due to the fundamental limit of aperture jitter in electronics (0.5-2 ps RMS [25]) and its impact on SNR, sub-sampling architectures have seldom operated above a few GHz.

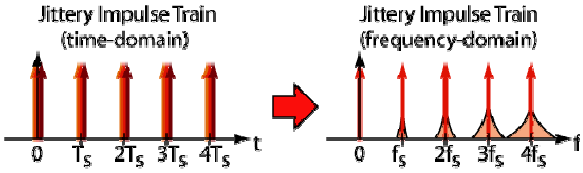


Figure 15: Increasing noise skirts at local oscillator harmonics arising from jitter in the time domain

Harmonic (GHz)	SNR (dB)	# of Bits
1	84	14.0
5	70	11.7
10	64	10.7
20	58	9.7
40	52	8.7

Table 1: SNR at different harmonic frequencies for a mode-locked laser with 10 fs RMS jitter

To examine the achievable performance of the proposed structure, consider that the SNR for a given aperture jitter and carrier frequency is described by [29]:

$$SNR = 20\log\left(\frac{1}{2\pi f \Delta t}\right) \tag{2}$$

where f is the carrier frequency and Δt is the RMS jitter of the local oscillator. Aperture jitter of mode-locked lasers have been shown to be extremely low (10-15 fs [30]), which facilitates the sub-sampling of RF signals in the 10's of GHz range with close to 8 bit precision. Furthermore, the high-Q (approximately 300) of the resonant optical phase modulator results in high suppression of any noise-folding effects. Table 1 lists the SNR values for various RF carrier frequencies assuming 10 fs RMS aperture jitter and a 2 MHz BW. Indeed, 8-bit resolution is possible at 40 GHz.

We have taped out a test chip to validate the above architecture, and expect to begin measurements of the overall system (which includes external optical components) in early 2006. Our target goal for this first prototype is to demonstrate 10-bit accuracy across a 2 MHz bandwidth with a 2 GHz carrier frequency and 200 MHz sample rate (i.e., repetition rate of the mode-locked laser).

7. INTEGRATED FEMTOSECOND LASERS

The passively mode-locked laser generating the low jitter sampling pulses does not necessarily need to be part of the ADC-Chip. Pulses could be easily generated externally and a fiber could be used for chirping as shown in Figure 1. However, if EPIC-chips with functionality based on the low-jitter properties of ultrafast lasers want to achieve a large penetration of all high-speed signal processing applications, the pico- or femtosecond lasers must be cheap, compact and integrated on the same platform. Such sources can also be used in a wide range of applications beyond the sampling application discussed here, such as a multi-wavelength laser source, feeding multiple channels of the communications system with appropriate filtering of the spectra and optical clock distribution to name only a few. For ultrashort pulse generation a saturable absorber is needed. A robust and reliable mode-locking mechanism can be achieved by saturable Bragg reflectors (SBRs) that provide diminishing loss for increasing intensity. Especially for very high repetition rate fundamentally mode-locked lasers [31], generating pulse trains at tens of GHz repetition rate, SBR's are currently the only compact saturable absorbers that can be employed for mode locking. For the gain material of an integrated modelocked laser, Er/Yb-waveguides deposited on Si/SiO_2 wafers (already used as inline amplifiers for planar light wave circuits) can be used. Here, we report on the first steps towards such an integrated laser source. Recently, we have demonstrated an SBR based on silicon, germanium, and silicon dioxide, and we demonstrated its

performance by mode-locking an Er-Yb:glass laser spanning the C-band [31]. The silicon/germanium SBR (Si/Ge-SBR) is integratable with both silicon and Er-Yb:glass, can be fabricated in a fully CMOS compatible process, and therefore offers the potential for highly compact, fully integrated and mass producible mode-locked lasers.

The Si/Ge-SBR demonstrated consists of a silicon/silicon-dioxide (Si/SiO_2) Bragg reflector and a germanium saturable absorber layer (Figure 16(a)). Due to the high refractive index contrast (n_{SiO2} = 1.45 and n_{Si} = 3.5), six layer pairs in the Bragg mirror are sufficient to achieve a reflectivity of 99.8%. On top of the Si/SiO_2 Bragg stack, a germanium saturable absorber layer is embedded in a silicon layer of $3\lambda/4$ optical thickness. It resides at a peak of the standing wave pattern of the electric field to maximize absorption and minimize saturation intensity (Figure 16(a)).

The fabrication of the Si/Ge-SBR was aimed at achieving both a high reflectivity of the Bragg mirror and a sufficiently strong nonlinear response of the absorber layer. The 6-pair reflector was deposited on a silicon-on-insulator (SOI) wafer (Figure 16b, step 1) and bonded with a new silicon substrate (Figure 16(b), step 2). Then, the silicon handle and buried oxide of the SOI-wafer were chemically etched to expose the crystalline silicon layer of the SOI-wafer (Figure 16(b), step 3). Subsequently, a 40 nm-thick germanium saturable absorber layer was epitaxially grown by the UHV-CVD technique developed by Luan *et. al*. [23] (Figure 16(b), step 4). Finally, a thin oxide was deposited on germanium as a passivation layer and then a poly-Si cap layer was deposited. This fabrication process results in the reversal of the Si/SiO_2 layer sequence of the reflector with respect to layer growth. Thus, the layers of lowest surface roughness – those that have been grown first – are located topmost in the mirror, and exposed to the highest electric field strength. In contrast, the rougher layers, grown last, are buried deep in the mirror (Figure 16(a)). This reversal of the layer sequence significantly reduces surface roughness and scattering losses. It therefore allows the $Si/Si0_2$ mirror to reach a reflectivity of 99.8%. Furthermore, this fabrication process terminates the reflector with the silicon layer of the SOI-wafer. The crystalline nature of this silicon layer preserves the optical absorption properties of the 40 nm-thick germanium layer and allows saturable absorption in the silicon / germanium material system at 1550 nm.

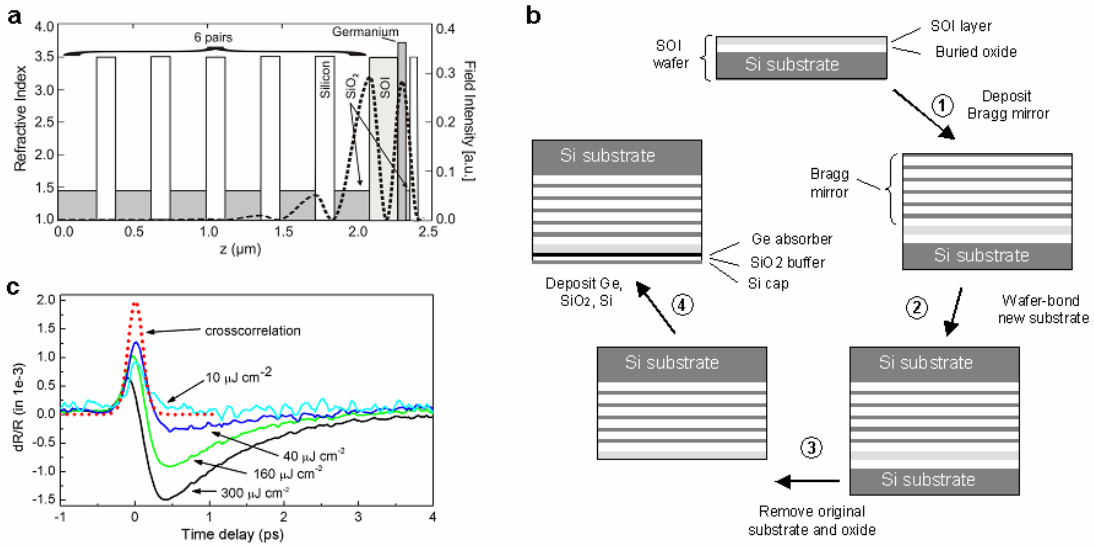


Figure16: (a) Structure and field distribution in the Si/Ge-SBR. (b) Fabrication process and (c) pump-probe traces taken at various fluence values (solid) along with the cross-correlation of the laser source (dashed).

The nonlinear response of the Si/Ge-SBR was characterized by pump-probe measurements with 150 fs pulses centered at 1540 nm. For low to medium fluence values (*e.g.* 40 $\mu J/cm^2$), the germanium layer acts as a fast saturable absorber with up to 0.13% of modulation depth (Figure 16(c)). The bleaching recovers on a sub-picosecond time-scale, with the temporal resolution of our measurement being limited by the pump and probe pulse durations. We attribute the fast sub-picosecond recovery time to intervalley scattering into the conduction band minima. In contrast, for high fluences (*e.g.*, 300 $\mu J/cm^2$), carriers generated by two-photon absorption (TPA) induce free carrier absorption (FCA) and turn the germanium layer to an inverse saturable absorber. The observed behavior leads to dual functionality of the Si/Ge-SBR in a mode-locked laser: (i) the fast recovery enables ultrashort pulse generation and broadband operation of the laser, (ii)

onset of inverse saturable absorption at high fluences helps stabilize lasers at high repetition rates against Q-switching [33,34]. This instability is especially pronounced in laser media with long upper state lifetimes such as Er-Yb:glass. It has prevented successful mode-locked operation of high repetition rate lasers until recently [31,33] and constitutes a major obstacle for compact laser integration. However, the inverse saturable absorption observed in the germanium layer counteracts the Q-switching instability by adding a passive feedback mechanism to the laser, which restores stable mode-locked laser operation.

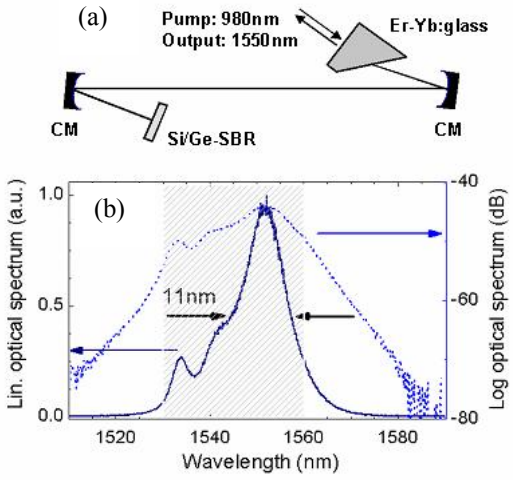


Figure 17: (a) Schematics of the laser cavity. (b) Optical spectrum of the Er-Yb:glass laser mode-locked with the Si/Ge-SBR on linear and logarithmic scale.

To demonstrate the performance of the Si/Ge-SBR we mode-locked a bulk Er-Yb:glass laser with this saturable absorber. The laser consists of a four-element laser cavity and operates at 169 MHz (Figure 17(a)). The fast recovery time of the Si/Ge-SBR combined with its high reflectivity leads to superior spectral width and pulse duration of the laser. We obtained an optical spectrum centered at 1550 nm with a full-width half-maximum (FWHM) bandwidth of 11 nm, that covered the entire C-band of optical communications at approximately –10 dB level (Figure 17(b)). After dechirping the pulses extracavity, the inferred pulse duration from the intensity autocorrelation is 212 fs. No Q-switching instability was observed in the laser regardless of pump power level despite the long upper-state lifetime and the small emission cross-section of the gain medium. We attribute the high stability against Q-switching to the inverse saturable absorption in the Si/Ge-SBR at high fluence.

After the successful development of a CMOS compatible saturable absorber further work is directed towards characterization of Er-doped waveguides and its properties when integrated with the Si/Ge-SBR.

8. CONCLUSIONS

Integration of HIC optical devices on the Si-Technology platform together with electronics may lead to advanced signal processing capabilities in the near future. In this paper, we discussed the key components of such a system such as filter banks, modulators, detectors, on-chip modelocked lasers as well as novel sampling techniques. Progress in the design and fabrication of these devices shows that device performance can meet the requirements for an optical analog-to-digital converter chip that may overcome the electronic bottleneck present in today's pure electronic sampling systems. Integration of these devices in a CMOS compatible process is pursued together with MIT Lincoln Laboratory.

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