An Interior-Ridge Silicon Microring Modulator

Erman Timurdogan, *Student Member, IEEE*, Cheryl M. Sorace-Agaskar, Ehsan Shah Hosseini, *Member, IEEE*, and Michael R. Watts, *Member, IEEE*

(Invited Paper)

***Abstract*—We design and demonstrate a new microring modulator geometry utilizing low-resistance interior ridge contacts and a hard outer waveguide wall to achieve high-speed operation in a device with a large free spectral range (FSR). The depletion-mode silicon microring modulator utilizes a hybrid vertical–horizontal junction to maximize the frequency response for a given voltage within a compact 2.5 μm radius. The 2.5-μm radius microring modulator demonstrates low energy (4.5 fJ/bit) error-free (bit error rate $<10^{-12}$) operation for 30 Gb/s nonreturn-to-zero data transmission without utilizing preemphasis or equalization. The modulator exhibits single mode operation over a wide, uncorrupted FSR of 5.3 THz, the largest reported in a high-speed ($>$25 Gb/s) modulator. The resulting combination of high-speed, low-energy operation, and a wide FSR offers the potential for very high bandwidth densities in future femtojoule-class communication links.**

***Index Terms*—Diodes, optical modulation, resonators, silicon.**

DESPITE the predictions of its demise, Moore's law scaling of transistor density [1] continues unabated with the recent introduction of 14 nm-node processes [2]. With die size remaining constant, the continued exponential growth in transistor count drives the communication requirements both on and off the chip at the same exponential growth factor, resulting in a doubling of the communication requirements every two years. This strain is felt most severely in the large server processors and high port-count switches within high performance computing platforms [3]. To handle the massive data flow, recently deployed systems have shifted to optical off-chip communications utilizing vertical cavity surface emitting lasers (VCSELs) both at the microprocessor and switch chip interfaces [4]. However, VCSELs provide only a single optical channel per fiber, and with exponential scaling, this limitation has led to a phenomenal growth in fiber-count and a resulting cabling problem that cannot be resolved with VCSEL-based serial communications. Wavelength division multiplexed (WDM) communications is required in future high performance computers.

Silicon photonics offers a unique combination of high-index-contrast waveguides in an active platform that provides CMOS-compatible dense integration of multiple channels within a single-mode system for wavelength-division-multiplexing (WDM) [5], [6]. Combined with CMOS integration, dense and seamless communications between the electronic and photonic layers are also possible [7], [8]. Close integration of CMOS logic with photonic communications has also led to the potential for dramatic improvements in communications energy efficiency, a secondary, but rather critical requirement for bandwidth scaling to continue at its present pace. These dual requirements have led to a drive to reduce the power consumption of each of the components that make up a silicon photonic communications link, from the laser sources to the modulators [9]–[20], filters [22]–[24], and detectors [25] required to implement a full link. Particular attention has been paid to modulator power consumption due to an early identification of the modulator as a potential high-power component, a result of the rather weak free-carrier plasma dispersion effect that represented the clearest path to an integrated silicon modulator [26]. Early work focused on the use of an electrical *p-n* junction diode placed inside a silicon waveguide to tune the phase of one or both arm(s) of a Mach–Zehnder (MZ) interferometer. MZ modulators have enabled wide-band and temperature insensitive operation [9]–[11], but the relatively weak plasma dispersion effect meant long structures ($>$500 μm) with large capacitance and high-power consumption. A compelling solution to the weak free-carrier response was to enhance the effect through the use of optical resonance, in compact microring modulators [12]. The first such modulators [12] relied on carrier injection which provide a large frequency shift due to the high carrier density introduced with an applied voltage. However, injection-based devices exhibit relatively low bandwidths due to the long free-carrier lifetime displayed on silicon-on-insulator (SOI) platforms. To increase the device speed, depletion-based modulators, primarily limited to the device electrical *RC* time constant, were introduced soon after the initial microring-modulator demonstration [13]–[20]. And, with the use of compact tightly confined vertical junction devices, extremely low power consumption has been achieved [13], [16]–[20].

With the introduction of depletion-based microring [14] and microdisk modulators [13], a path has been identified to achieve high-speed and ultralow power dense WDM communications on a silicon platform. However, whispering gallery-mode resonators suffer from the presence of multiple modes and the corresponding spurious (e.g., high-order) resonances deteriorate the available free-spectral-range (FSR). The FSR, or separation between resonances, of the modulator is a critical parameter since it sets the available optical bandwidth of the communication line. The FSR should be as wide as possible to enable the maximum channel count on a given communication line.

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The authors are with the Research Laboratory of Electronics, Massachusetts Institute of Technology, Cambridge, MA 02139 USA (e-mail: ermant@mit.edu; ch20117@mit.edu; ehsansh@mit.edu; mwatts@mit.edu).

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In microring modulators, the traditional ridge-waveguide-based contacting geometry limits the minimum bend radii since it sets up a radiation path via the remaining exterior silicon slab. Given that the FSR between azimuthal modes is inversely proportional to the radius, the ridge-waveguide contacting geometry limits the FSR in microring modulators. The use of a vertical junction design enabled the use of interior electrical contacts and a step index outer wall that dramatically reduced the size of the resonator and opened up the possibility for a very wide FSR. However, the microdisk resonators that have formed most of these demonstrations [13], [16], [17] support higher order radial modes, which still corrupt the available FSR. The effect of these radial modes can be eliminated through the use of a propagation-constant-matched coupling region [19], [21] at the expense of relatively small electrical bandwidth due to large radius or an adiabatic bend implemented within the microring to enable simultaneous interior electrical contact and single-mode wide FSR operation [18], [22]. However, adiabatic resonant microring (ARM) modulators impose a tradeoff between the modulator electrical bandwidth and the electro-optic response due to the excess resistance introduced by the contact geometry.

In this paper, we address this limitation by introducing a new modulator geometry, which enables both a large electrical bandwidth and a wide-FSR through the use of an interior ridge contact. Furthermore, we introduce a hybrid vertical–horizontal junction that achieves a large free-carrier depletion or accumulation response of the microring for a given applied voltage while maintaining interior contacts and a step index hard outer wall. The modulator's hard outer wall supports high-Q single mode operation over a wide uncorrupted FSR of 5.3 THz (>50 channels) in a 2.5 μm radius interior ridge resonator. The modulator demonstrates a large electro-optic shift (up to 8 GHz/V), low energy-per-bit operation (4.5 fJ/bit), high-speed (30 Gb/s), and error-free data transmission. Together these advances illustrate the potential of silicon photonic microring modulators for achieving multiterabit/s communication lines.

I. Modulator Design

A. Depletion-Mode Junction Optimization

In depletion (or accumulation) modulators, the applied voltage to a *p-n* junction induces a change in the depletion width, which results in a perturbation to the permittivity ($\Delta\varepsilon$) of silicon imposed by the plasma-dispersion effect [26]. The perturbation to the permittivity induces a resonant frequency shift, $\Delta\omega_m$ of each mode m, which can be derived from Poynting's theorem [27] and is expressed in (1) as the ratio between the perturbed and total energy within the resonator.

$$\Delta\omega_m = \frac{-\frac{\omega_m}{4}\Delta\varepsilon\int_{v_p} e_m^* \cdot e_m\, dv}{\frac{1}{2}\varepsilon\int_{v_o} e_m^* \cdot e_m\, dv} \approx -\frac{\omega_m}{2}\frac{\Delta\varepsilon}{\varepsilon}\frac{v_p}{v_o} \qquad (1)$$

where ε is the permittivity of silicon, ω_m is the unperturbed resonant frequency, and e_m is the electric field distribution of the mode number m, while ν_p and ν_o are the perturbed and total resonator volume, respectively. The electric field, e_m, is assumed to have a uniform flattop distribution within the silicon core for achieving the approximation in (1). The total resonator volume can be also approximated as $\nu_o = \mathrm{WHL}$, where W, H, and L are the width, height, and length of the resonator core, respectively. The perturbed volume is related to the junction profile and the change in depletion as follows, $\nu_p = \Delta w_d \mathrm{DL}$, where Δw_d is the change in depletion region for a given applied potential, D is the junction profile dependent parameter, shown in Fig. 1(a), and L is the length of the resonator. D is equal to H, W for lateral [14] and vertical [13], [16]–[18] junction profiles, respectively, and is equal to the ratio of the core area (HW) and the length of the *p-n* junction period $(L_{p\text{-}n})$, $2\mathrm{HW}/L_{p\text{-}n}$ for an interleaved junction profile [15], [19]. The ratio of the change in permittivity $(\Delta\varepsilon)$ to the permittivity (ε) can be related to the change in refractive index (Δn) to the refractive index by $\Delta\varepsilon/\varepsilon = ((n+\Delta n)^2 - n^2)/n^2 \approx 2\Delta n/n$. Using the derived expressions, the resonant frequency shift is simplified as

$$\Delta\omega_m = -\omega_m \frac{\Delta n}{n}\frac{\Delta w_d D}{\mathrm{WH}}. \qquad (2)$$

Further, the change in refractive index (Δn) is related to acceptor and donor free-carrier concentrations by the plasma-dispersion effect, and is expressed in (3) based on a curve fit [13] to the experimental data from [26].

$$\Delta n = A_{A,D} N_{A,D}^{B_{A,D}} + jC_{A,D} N_{A,D}^{D_{A,D}} \qquad (3)$$

where N_D and N_A are the donor and acceptor concentrations, respectively, and the curve fitting parameters $A_D = -2.37 \times 10^{-23}$, $\mathrm{B}_D = 1.08$, $C_D = 4.92 \times 10^{-26}$, $D_D = 1.2$, and $A_A = -3.93 \times 10^{-18}$, $B_A = 0.82$, $C_A = 1.96 \times 10^{-24}$, $D_A = 1.1$ are used for donors and acceptors, respectively. It

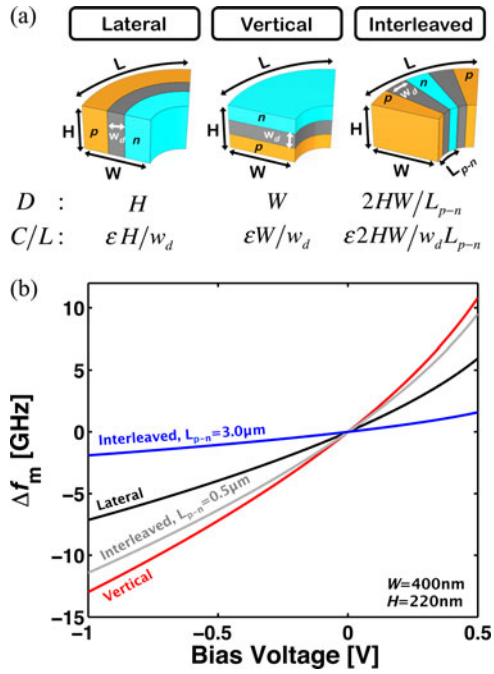


Fig. 1. (a) Lateral, vertical, and interleaved junction profiles for common depletion-mode modulators. Junction profile dependent parameter (D) and capacitance per unit length (C/L) is depicted below each junction profile. (b) Frequency shift based on (2), (3), and (6) as a function of applied potential for a fixed silicon core width of 400 nm and height of 220 nm for three different junction profiles.

is important to note that the imaginary part of index change is not inducing a real frequency shift, but changing the loss within the cavity. Therefore, the real part of the index change in (3) of both acceptors and donors can be related to the frequency shift in (2). Assuming $B_A \approx B_D \approx 1$, $A \approx A_A \approx A_D$ and $N_A \approx N_D \approx N$ for the sake of simplicity, the frequency shift can be further simplified as

$$\Delta\omega_m = -\omega_m \frac{\mathrm{AN}\Delta w_d}{n}\frac{D}{\mathrm{WH}}. \tag{4}$$

Furthermore, the frequency shift can be related to the depleted or accumulated charge (ΔQ) per unit length, $\Delta Q/L = qND\Delta w_d$, where q is the electronic charge. The depleted or accumulated charge can be also approximated as $\Delta Q \approx C\Delta V = CV_{\mathrm{pp}}$ for $\Delta w_d \ll w_d$, where, V is the applied electric potential and C, equal to $\varepsilon DL/w_d$, is the junction capacitance. The simplified frequency shift expression is written as

$$\Delta\omega_m \approx -\omega_m \frac{A}{nq}\frac{\mathrm{CV}}{\mathrm{WHL}} = -\omega_m \frac{A}{nq}\frac{\mathrm{CV}}{\nu_o}. \tag{5}$$

We conclude based on (5) that the frequency shift ($\Delta\omega_m$) of a depletion modulator is directly proportional to the capacitance per unit volume of the resonator (C/v_o). Since the waveguide core (e.g., width and height) is generally fixed for achieving single mode operation, it is desirable to maximize the junction capacitance per unit length to achieve the largest frequency shift for a given applied voltage in depletion-based modulators. It is important to note that the depletion width and junction capacitance are a function of the applied potential. The approximated depletion width for an abrupt *p-n* junction as a function of voltage is given in (6) [28], assuming $N_A \approx N_D \approx N$,

$$w_d \approx 2\sqrt{\frac{\varepsilon}{q}\frac{V+\phi_B}{N}} \tag{6}$$

where ϕ_B is the built-in potential. While the increased capacitance might appear to increase the switching energy (CV^2), the reduction in the voltage required to achieve a desired frequency shift outweighs this effect due to the square-dependence of the voltage on the switching energy.

Moreover, attaining a CMOS compatible voltage ($\sim$1V) is itself an important parameter and a higher capacitance reduces the drive voltage. It is important to note that only the junction capacitance that interacts with the optical mode matters, capacitance elsewhere in the device should be minimized.

Generally, depletion-based modulators can be classified into lateral [14], vertical [13], [16]–[18], and interleaved [15], [19] junction profiles [see Fig. 1(a)] or a combination of the three [20]. Silicon waveguides have taken on a wide but thin profile in order to reduce the susceptibility of the waveguide to lithographic variations, minimize the aspect ratio of gap fills, and to ensure polarization-maintaining operation. On account of this aspect ratio, vertical junction modulators achieve a greater capacitance per unit length than horizontal junction modulators and therefore achieve lower voltage and energy consumption operation [16], [19]. However, an interesting horizontal junction modulator design has emerged [15], commonly referred to as the interleaved junction. Interleaved junctions can achieve a very large capacitance per unit length, and can even surpass the performance of the vertical junction modulator if the *p-n* junction period ($\mathrm{L}_{p\text{-}n}$) is such that $\mathrm{L}_{p\text{-}n} \leq 2$ H (e.g., <400 nm). However, to achieve such a tight pitch requires high-resolution implant mask features (<150–200 nm) and contact-to-contact spacing (<300 nm) which may not always be compatible with a given silicon photonics process flow.

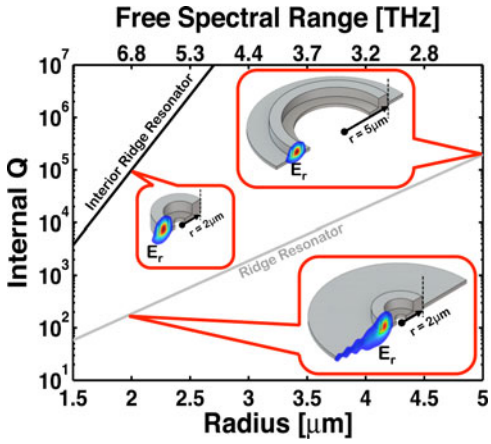


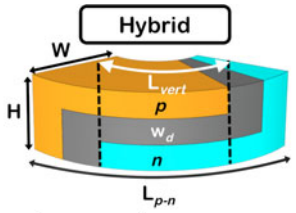
Fig. 2. Quality factor scaling as a function of radius and FSR for ridge and interior ridge resonators. TE_0 radial electric field mode profile of important points is overlaid with the resonator cross-section. Ridge resonator has full and ridge thickness of 300 and 80 nm, respectively. Interior ridge resonator has full and ridge thickness of 220 and 110 nm, respectively.

To illustrate the differences between each junction profile, the resonant frequency shift as a function of voltage is obtained using (2), (3), and (6), and depicted in Fig. 1(b) at $\lambda = 1.55$ μm for a fixed core thickness of 220 nm, width of 400 nm, a built-in potential of 0.7 V, and a carrier concentration of $10^{18}/\mathrm{cm}^3$. As is shown in the graph, the vertical and interleaved junction profiles provide the greatest frequency shift for a given applied voltage.

B. Compact Single-Mode Resonator Design

The resonator design is as important to the energy consumption as the junction design since a smaller resonator can achieve a lower overall capacitance without altering the capacitance per unit volume, leading to a high electrical bandwidth ($\mathrm{f}_{3\mathrm{dB}} \sim 1/2\pi\mathrm{RC}$) and high-speed operation. Additionally, the smaller the resonator the larger the FSR and available optical bandwidth for WDM communications. Since the FSR is inversely proportional to the radius, an optimized resonator for WDM operation requires tightly confined compact resonators. Additionally, the resulting resonator must exhibit a high radiation limited quality factor ($>10^5$) since the frequency shift of the modulator is generally small.

Ridge-waveguides enable straightforward contact to microrings by utilizing exterior and interior contacts and represent a large class of silicon microring modulators. In [14], a 300 nm tall, 480 nm wide waveguide with a ridge thickness of 80 nm was utilized and achieved the most compact ridge-based modulator to date. However, when simulating the internal quality factor of this resonator with a finite difference cylindrical mode-solver (FDM) [29], the quality factor (Q) as a function of radius ($\lambda \sim 1.55$ μm), plotted in Fig. 2 reveals that a $Q \sim 10^5$ is only achieved for $\sim$5 μm bend radius. Therefore, this geometry



$$D:\left(L_{vert}/L_{p-n}\right)\times W+2HW/L_{p-n}$$
$$C/L:\left(\varepsilon/w_d\right)\times\left(\left(L_{vert}/L_{p-n}\right)\times W+2HW/L_{p-n}\right)$$

Fig. 3. Hybrid Junction profile for single *p-n* junction period and corresponding overlap and capacitance per unit length.

limits the FSR to only ~2.4 THz and simultaneously increases the capacitance unnecessarily.

In contrast, if we use an interior ridge contact, and step-index outer wall, we can achieve a radiation limited internal Q of 10^5 for an intrinsic silicon interior ridge microring with a ~2 μm bend radius corresponding to an FSR of 6.8 THz (e.g. ~68 channels at 100 GHz channel-to-channel spacing) even with a silicon thickness of only 220 nm. While a radiation limited Q of 10^5 is roughly an order of magnitude higher than what is required in the final structure, in an optimally designed device, the free-carrier losses limit the radiation Q so as to ensure the highest speed and largest frequency shift for a given applied voltage. The resulting resonator exhibits a volume and capacitance that is reduced by at least a factor of 6.25 over prior high-speed microring modulators demonstrations [14], [15] even for the same junction design. A WDM link, formed by interior ridge resonators, can achieve unprecedented channel (~68) and on-chip bandwidth (e.g. 2.4 Gb/s/μm^2 at a data rate of 30 Gb/s per channel) density, and can be transmitted/received by a single mode waveguide and fiber (~2 Tb/s/fiber).

II. Single Mode Interior Ridge Modulator

A. Interior Ridge Modulator Design

Although a compact interior-ridge resonator allows for single mode high-Q ($>10^5$) operation, it only enables direct contact to the interior ridge for the bottom half of the waveguide. Thus, a vertical junction alone will not be able to have interior contacts, but an interleaved junction or a vertical-interleaved hybrid junction facilitates contact within an interior-ridge resonator. The hybrid junction enables further optimization of the capacitance per unit length (C/L) shown in Fig. 3, by simply adjusting the ratio of vertical junction length $(L_{\rm vert})$ and the *p-n* junction period $(L_{p\text{-}n})$ and can achieve a high capacitance per unit length while reducing the required lithographic resolution. In order to minimize the contact resistance, the hybrid junction is contacted through the interleaved interior $p+$ and $n+$ doped regions, formed next to the ridge edge, as shown in Fig. 4(a).

The identical *p*- and *n*-type doping concentrations were simulated using Sentaurus Process to have a depletion width (w_d) of 120 nm to achieve optimum balance between internal Q, the modal overlap, and junction capacitance. The $p+$ and $n+$ type doping concentrations are targeted for more than 5×10^{19}/cm^3 to minimize contact resistance. In order to implement the modulator, two levels of metal were used to avoid shorting of the

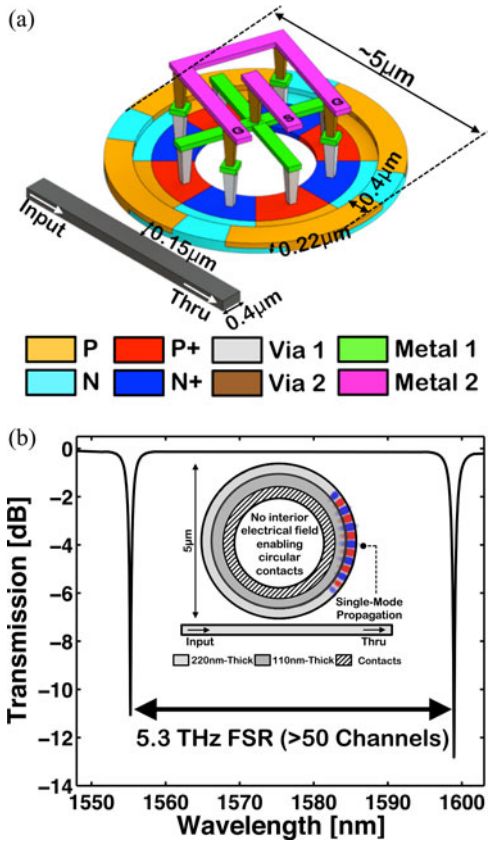


Fig. 4. (a) 3-D sketch of the designed and fabricated interior ridge electro-optic silicon modulator and bus waveguide, showing size, implants, and metal interconnection. (b) 3D-FDTD simulation of an interior ridge resonator, showing single-mode operation and almost loss-less (>99.9%) circular interior contacts.

n and p contacts to the diode [see Fig. 4(a)]. The junction period was chosen to be 3.6 μm due to interior contact-to-contact spacing limitations within our fabrication process, but the ratio of the vertical component of the junction to the total junction length was varied according to $L_{\rm vert}/L_{p\text{-}n}=0$, 0.25, 0.5, respectively, (see Fig. 3), resulting in a capacitance per unit length of 0.05, 0.13, and 0.22 fF/μm and corresponding estimated frequency shifts of 1.9, 5.0, and 8.3 GHz/V for each junction. An $L_{\rm vert}/L_{p\text{-}n}$ above 0.5 would improve the frequency shift for a given applied voltage in the device, but at the expense of reduced electrical bandwidth as a result of increased resistance within the hybrid junction.

The resonator with the interior ridge contact previously described, was implemented using a conservative 2.5 μm outer radius with an interior-ridge etch. Three-dimensional finite difference time domain (FDTD) ring-down simulations were performed in order to verify that the structure was in fact single mode and to assess the resultant FSR. A top-view of the radial electric field mode distribution, depicted in Fig. 4(b) (inset), clearly demonstrates that only one radial mode was excited. The spectral response of the ring, obtained from discrete Fourier transforms of the FDTD simulations with the results plotted in Fig. 4(b), revealed the expected 5.3 THz FSR.

B. Interior Ridge Modulator Fabrication and Results

The rigorously designed and simulated interior ridge modulator was fabricated in a 300 mm CMOS foundry using

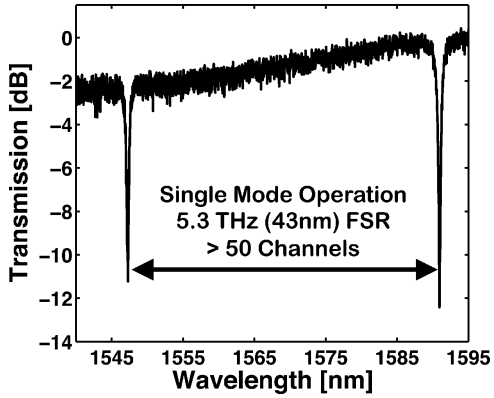


Fig. 5. Transmission (through port) spectrum of a 2.5 μm radius interior ridge resonator, showing single mode operation over a 5.3 THz (43 nm) FSR.

silicon-on-insulator (SOI) wafers with a 225 nm top silicon layer and 2-μm buried oxide (BOX) layer for optical isolation. A full silicon etch was applied to form the resonator and bus waveguide. A partial timed silicon etch was then applied to form the interior ridge with a thickness of 115 nm. An oxidization step followed to passivate the sidewalls, which decreased the full and partial waveguide thickness to 220, and 110 nm, respectively. The hybrid *p-n* junction, centered at ~110 nm thickness, was formed from arsenic (As) and boron difluoride (BF_2) implants. The interior $n+$ and $p+$ doped regions were formed by phosphorus and BF_2 implants. Low resistance interior vias were contacted to highly doped regions by self-aligned silicidation. Finally, the contacts were connected to on-chip ground-signal-ground (GSG) probing pads by two levels of copper wiring and contact layers [see Fig. 4(a)].

The spectral response of the modulator was measured by exciting the fundamental TE-mode of the bus waveguide with an Agilent 81600B tunable laser source. The laser was tuned from $\lambda \sim 1543$ nm to $\lambda \sim 1595$ nm and the resulting measured spectrum, shown in Fig. 5, demonstrates single-mode operation over a wide uncorrupted FSR of 5.3 THz.

In order to experimentally demonstrate the advantage of a hybrid junction profile, interior ridge modulators with different vertical junction and interleaved junction ratios ($L_{\rm vert}/L_{p\text{-}n} =$ 0, 0.25 and 0.5) were fabricated. A vertical junction microdisk modulator, published elsewhere [15], was used for comparison. All modulators were tuned individually by applying voltage across the modulator contacts and the frequency shift of each modulator as a function of voltage is shown in Fig. 6(a). The vertical junction microdisk modulator has an 11 GHz/V frequency shift, whereas, the hybrid junction interior ridge modulator has a 2, 5, and 8 GHz/V frequency shift for $L_{\rm vert}/L_{p\text{-}n} = 0$, 0.25 and 0.5, respectively. The realized modulator frequency shifts are in line with the previously estimated frequency shifts based on the design in Section II-A. The minor discrepancy can be attributed to the nonideal junction profile and modal overlap with the depletion width. The interior ridge hybrid junction modulator, $L_{\rm vert}/L_{p\text{-}n} = 0.5$, achieved only ~1.3 times smaller frequency shift or capacitance per unit length, which in turn required ~1.3 times more voltage than a vertical junction modulator. However, the length of the *p-n* pairs ($L_{p\text{-}n}$) can be minimized to induce much larger frequency shifts for a given applied voltage.

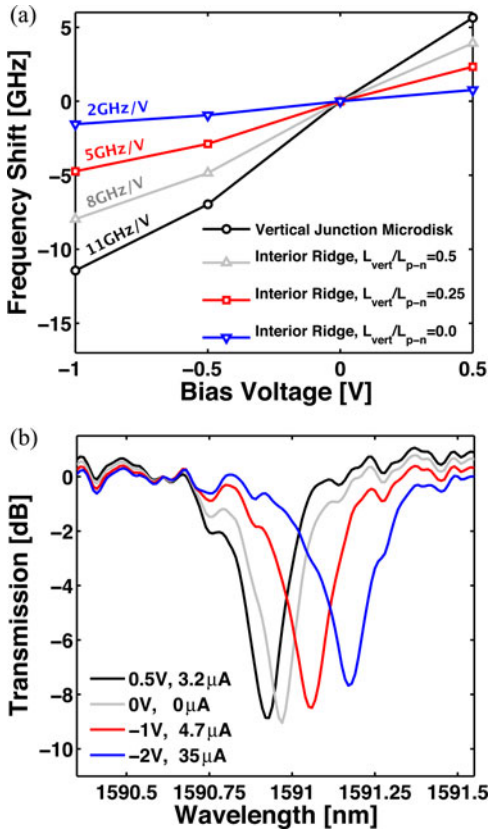


Fig. 6. (a) Measured electro-optic resonance frequency shifts for vertical microdisk and interior ridge modulators ($L_{\rm vert}/L_{p\text{-}n} = 0$, 0.25 and 0.5). (b) Measured transmission spectra of the resonator at applied dc bias voltages of 0.5, 0, –1, and -2 V, respectively.

The spectral response as a function of applied dc bias for $L_{\rm vert}/L_{p\text{-}n} = 0.5$ is shown in Fig. 6(b). The internal Q was limited to ~8000 by the nonzero overlap of the optical mode and interior highly doped $p+$ and $n+$ regions, separated by only 300 nm from the interior edge of ridge. Those regions can simply be placed further from the ridge edge to achieve higher internal Q. The modulator was also slightly overcoupled, which limited the static extinction ratio to ~9 dB. This can also be improved by properly adjusting the gap between the modulator and bus waveguide to achieve critical coupling.

C. High Speed Characterization

A high-speed pattern generator was used to generate a non-return-to-zero (NRZ) on-off-keyed (OOK) signal, encoded with a 2^{31}–1 pseudo-random-bit-sequence (PRBS) at data rates from 15 to 30 Gb/s. The output of the pattern generator was 0.5 $V_{\rm pp}$ with a 0.25 V reverse dc bias. A dc bias-tee and a linear amplifier were used to achieve a voltage swing from 0.5 V to -1.7 V (2.2 $V_{\rm pp}$). A 50 Ω-terminated GSG probe was used to eliminate transmission line reflections and ensure that the voltage dropped across the modulator was the driven 2.2 $V_{\rm PP}$. The lightwave, coupled into the interior-ridge modulator ($L_{\rm vert}/L_{p\text{-}n} = 0.5$), was set to $\lambda \sim 1590.9$ nm and the through port output passed through an erbium doped fiber amplifier (EDFA) to overcome

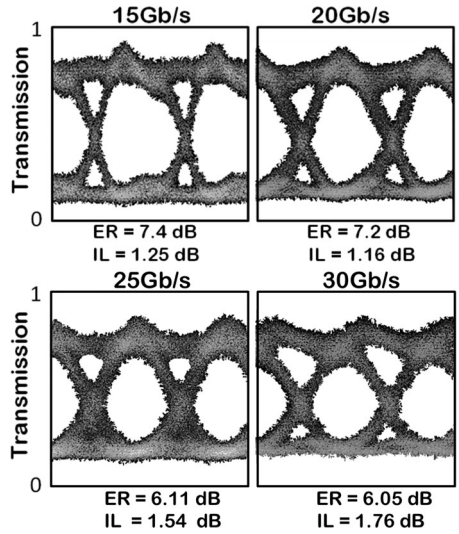


Fig. 7. Experimentally measured high-speed optical eye diagrams egressing from the silicon electro-optic hybrid junction interior ridge modulator ($L_{\rm vert}/L_{p\text{-}n} = 0.5$), which was driven with a terminated probe and 2.2 $V_{\rm PP}$ NRZ-OOK PRBS at a data rate of 15, 20, 25 and 30 Gb/s and a pattern length of a 2^{31}–1. Extinction ratio (ER) and insertion loss (IL) are denoted below the eye diagrams at each data rate.

fiber-to-chip coupling losses. A tunable bandpass filter with a 1 nm full-width-half-maximum was used to filter out the amplified spontaneous emission (ASE) of the EDFA.

High-speed optical eye diagrams were measured with a digital sampling scope at data rates of 15, 20, 25, and 30 Gb/s. The dynamic extinction ratio and insertion loss, shown below each eye diagram in Fig. 7, were calculated from the optical true "0" and true "1," indicated on the vertical axis. Optical true "0" and "1" correspond to the amplified spontaneous emission (ASE) floor after the filter and the off resonance transmission level at $\lambda \sim 1590$ nm, respectively. With low insertion loss ($\sim$1.8 dB) and high extinction ratio (6.1 dB) at a data rate of 30 Gb/s, the eye diagrams were continuously open at data rates from 15 to 30 Gb/s. Throughout the experiments, neither signal equalization nor preemphasis was used.

D. Signal Integrity Measurements

The data transmission encoded by the hybrid junction modulator ($L_{\rm vert}/L_{p\text{-}n} = 0.5$) was passed through a variable optical attenuator (VOA) and received by a 40 Gb/s high-speed *p-i-n* photodiode and transimpedance amplifier (PIN-TIA). The received data were then fed differentially to a bit-error-rate tester (BERT) for evaluation. The total fiber-to-fiber insertion loss was $\sim$16 dB, and the intensity before the EDFA was ~ -10 dBm.

Bit-error-rate (BER) measurements, shown in Fig. 8(a) and (b), were performed at data rates of 15, 20, 25, and 30 Gb/s, respectively. For all data rates, the device achieved error-free operation (BER $<10^{-12}$) for a PRBS pattern length of $2^{31}-1$. No pattern-dependence from 2^7-1 to $2^{31}-1$ was observed due to the low leakage currents and depletion-mode operation. A commercial $LiNbO_3$ Mach–Zehnder modulator, rated to a 3 dB bandwidth of 35 GHz, was similarly characterized for reference. The commercial modulator was driven with an ac coupled 5.5 $V_{\rm PP}$ electrical signal. The power penalty was recorded as the

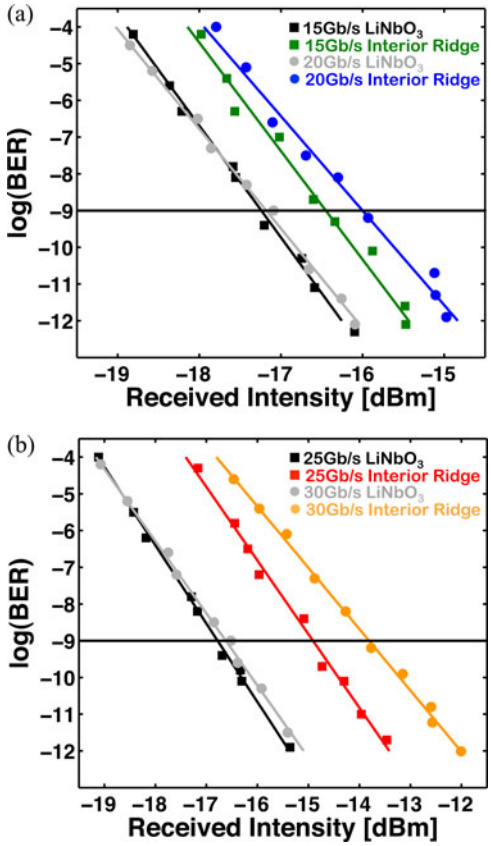


Fig. 8. Bit-error-rate (BER) curves measured for a silicon electro-optic hybrid junction interior ridge modulator ($L_{\rm vert}/L_{p\text{-}n} = 0.5$) and a commercial $LiNbO_3$ modulator at (a) 15 and 20 Gb/s data rates and (b) 25 and 30 Gb/s data rates, all with PRBS pattern lengths of a 2^{31}–1. The bit-error-rate curves for the commercial $LiNbO_3$ modulator were used as a reference to obtain the power penalty of the interior ridge modulator. Data transmission with the interior ridge modulator were received with a power penalty of 0.8, 1.18, 1.87, and 2.8 dB at data rates of 15, 20, 25, and 30 Gb/s, respectively.

received intensity (power) difference at a BER of 10^{-9} between the silicon hybrid junction interior ridge modulator and the commercial $LiNbO_3$ modulator [Fig. 8(a)]. Transmitted data were received with a power penalty of 0.8, 1.18, 1.87, and 2.8 dB at data rates of 15, 20, 25, and 30 Gb/s, respectively. The increasing power penalty with increasing data rate is related to the *RC* limited response of the modulator.

E. Energy Consumption

The energy consumption of the interior-ridge modulator ($L_{\rm vert}/L_{p\text{-}n} = 0.5$) was measured using a time domain reflectometer (TDR). The absorbed power by the GSG pads was subtracted from the absorbed power by the modulator. This normalization is required because with close CMOS integration, only the lower level metal wiring and contact wiring remains as part of the modulator itself. The pads themselves would not exist. This required two consecutive TDR measurements; one with pads only serving as a reference and one with the modulator, metal wiring, and pads. The experimental setup is shown in Fig. 9(a) for the reference and Fig. 9(b) for the modulator with pads. The reference reflected voltage (V_P^-) was measured by attaching the transmission line and the non-terminated GSG probes, landed

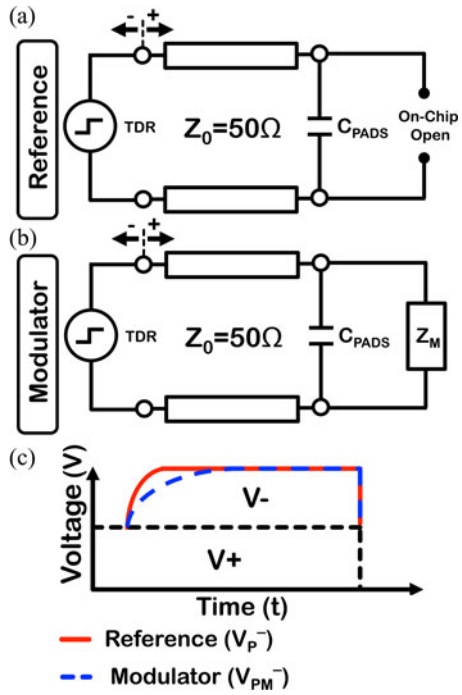


Fig. 9. Time Domain Reflectometer (TDR) measurement setup: (a) electrical setup, configured for measuring reflected voltage (V_P^-) from open ended on-chip pads (C_{PADS}), (b) electrical setup, configured for measuring reflected voltage ($V_{\mathrm{PM}}{}^-$), from modulator load (Z_M) and identical on-chip pads (C_{PADS}), (c) emanating TDR input (+ direction) and reflected TDR output (− direction) representation for reference and modulator with pads for a given voltage input.

on an on-chip set of open-circuit pads (C_{PADS}). The modulator with pads reflected voltage (V_{PM}^-) was also measured by attaching the transmission line and the non-terminated GSG probes, landed on an identical set of pads (C_{PADS}) connected to the modulator, which then serves as the load (Z_M). For a given TDR step input, the reference (V_P^-) and the modulator with pads (V_{PM}^-) reflected voltage is sketched in Fig. 9(c). Frequency domain reflection components for the reference (S_{11}^P), the modulator with pads (S_{11}^{PM}), and the modulator by itself (S_{11}^M) were expressed in (7), assuming $1/j\omega C_{\mathrm{pads}} > Z_0$, where, $Z_0 = 50\,\Omega$, is the characteristic impedance of the transmission line.

$$S_{11}^P = \frac{V_P^-}{V_{\mathrm{in}}},\ S_{11}^{\mathrm{PM}} = \frac{V_{\mathrm{PM}}^-}{V_{\mathrm{in}}}, S_{11}^M = \frac{S_{11}^{\mathrm{PM}}}{S_{11}^P} \tag{7}$$

where V_{in} is the input voltage emanating from the TDR. The absorbed switching power (P_s^M) was then calculated according to (8).

$$P_s^M = \left(1 - \left(S_{11}^M\right)^2\right) V_{\mathrm{in}}^2/Z_0. \tag{8}$$

Since the capacitance a function of voltage will slightly vary and the TDR step height is 0.25 V_{pp}, measuring power consumption requires multiple measurements; here five measurements were done from 0.5 to −2 V and a bias-tee was used to adjust the dc offset. Then, the total switching power (P_s^M) is integrated over time to obtain switching energy E_s, expressed in (9).

$$E_s = \int P_s^M\, dt. \tag{9}$$

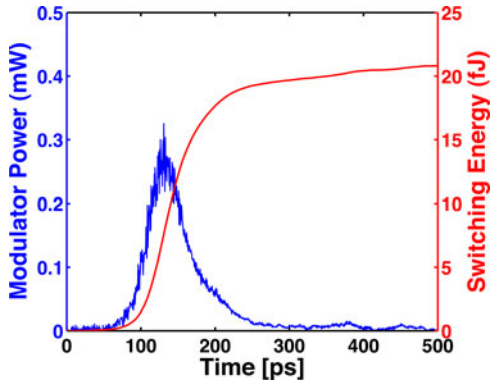


Fig. 10. Time domain reflectometry (TDR) measurement of the hybrid junction modulator power consumption and switching energy ($E_s = CV_{\mathrm{PP}}^2$) for a 2.5V_{PP} drive from 0.5V to −2.0V. The average capacitance is extracted to be 3.3 fF. The energy-per-bit for a 2.2 V_{PP} drive from 0.5 V to −1.7 V is ∼4 fJ/bit ($E_{\mathrm{bit}} = E_s/4 = 3.3$ fF $\times$ $2.2V_{\mathrm{PP}}^2/4 = 4$ fJ/bit).

The measured power consumption and switching energy are shown in Fig. 10 for a 2.5 V_{pp} with a dc bias of −0.75 V dropped across the modulator pins. The switching energy ($E_s \approx$ C $\mathrm{V}_{\mathrm{PP}}^2$) was experimentally extracted to be 20.8 fJ. Therefore, the average capacitance of the modulator was determined to be ∼3.3 fF.

In a PRBS-NRZ signal, transitions from 0 to 0, 0 to 1, 1 to 1, and 1 to 0 are equally probable and the energy is only consumed to charge the capacitor in a 0 to 1 transition. Therefore, the energy-per-bit consumption of the modulator is one quarter of the switching energy; here 4 fJ/bit for a 2.2 V_{pp} drive ($E_{\mathrm{bit}} = E_s/4 = 3.3$ fF $\times$ 2.2 $\mathrm{V}_{\mathrm{PP}}^2/4 = 4$ fJ/bit). The modulator also consumed 0.5 fJ/bit (19 μA $\times$ (1.7 V/2)/30 Gbits/s = 0.5 fJ/bit) due to a leakage current of 19 μA at −1.7 V, originating from band-to-band tunneling between interior interleaved $p+$ and $n+$ regions. The total energy-per-bit for the hybrid modulator was then 4.5 fJ/bit. The leakage current can be eliminated by introducing oxide trenches between the interior $p+$ and $n+$ regions.

III. Conclusion

By implementing an interior ridge-contacting scheme in a microring-modulator with a hard outer wall resonator design together with a vertical-interleaved hybrid junction, we have demonstrated a modulator that simultaneously achieves high-speed (30 Gb/s) operation and a large, uncorrupted FSR (5.3 THz). Specifically, the hybrid junction yields a frequency shift of 8 GHz/V, and enables 30 Gb/s error free operation with 2.2 V_{pp} terminated drive and 4.5 fJ/bit power consumption. Tight confinement enabled by the step index hard-outer resonator wall, an optimized modal overlap with the depletion region, low device capacitance, and high junction capacitance-per-unit-volume together enabled this result. Even with a relatively large channel-to-channel spacing of 100 GHz, this modulator can be used to achieve an unprecedented on- and off-chip bandwidth density of ∼1.5 Gb/s/μm^2 or 1.6 Tb/s/fiber (or waveguide), respectively. Additionally, the energy consumption and drive voltage of this modulator can be further minimized by simply increasing the internal Q and the number of interleaved *p-n* junction pairs within the modulator.

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Erman Timurdogan received the B.S. (Hons.) degree in electrical and electronics engineering from Koc University, Istanbul, Turkey, in 2010. He then joined the Photonics Microsystems Group, the Massachusetts Institute of Technology (MIT), Cambridge, MA, USA. He received S.M. degree in electrical engineering from MIT in 2013 in "Automated Wavelength Recovery for Silicon Photonics." He is currently a member of the Photonics Microsystems Group at MIT and working toward the Ph.D. degree.

He was with Mercedes-Benz Turk, Istanbul, Turkey, in 2008 and Bruker Optics, Karlsruhe, Germany, in 2009. His current research interests include modeling and testing integrated electro-optic and thermo-optic photonic devices and systems for low-power, high speed, wavelength division multiplexed (WDM) communications. He has more than 20 authored and coauthored conference and journal publications and an issued patent.

Mr. Timurdogan is also a member of the Optical Society of America (OSA).

Cheryl M. Sorace-Agaskar received the B.S. degree (Magna Cum Laude) in engineering physics from Cornell University, Ithaca, NY, USA, in 2008. She then joined the Optics and Quantum Electronics Group, the Massachusetts Institute of Technology Cambridge, MA, USA, where she received her S.M. degree in electrical engineering in 2010 for her thesis entitled "Advanced silicon photonic modulators." She is currently also a member of the Photonics Microsystems Group and is working toward the Ph.D. degree.

Her current research interests include modeling, testing, and design frameworks for integrated analog optics in a silicon platform.

Ms. Sorace-Agaskar is a member of the Optical Society of America (OSA).

Ehsan Shah Hosseini received the B.S. degree in electrical engineering from the Sharif University of Technology, Tehran, Iran, in 2003, and the M.S. and Ph.D. degrees in electrical engineering from the Georgia Institute of Technology, Atlanta, GA, USA, in 2008 and 2011, respectively. He is currently a Postdoctoral Associate in Photonics Microsystems Group, MIT.

His research interests include silicon photonics, biosensing, and solid state lasers.

Dr. Ehsan is a member of Optical Society of America (OSA).

Michael R. Watts received the B.S. degree in electrical engineering from Tufts University, Medford, MA, USA, in 1996, the S.M. and Ph.D. degrees from Massachusetts Institute of Technology (MIT), Cambridge, MA, USA, in 2001 and 2005, respectively.

He is an Associate Professor with the Department of Electrical Engineering and Computer Science (EECS) and a Principal Investigator in the Research Laboratory of Electronics (RLE) and at the MIT, where he leads the Photonic Microsystems Group. He then joined the Charles Stark Draper Laboratory as a Member of Technical Staff in their Fiber Optics Group. In 1999, he became a Draper Fellow in MIT. In 2005, he joined Sandia National Labs, where he led their silicon photonics effort as a Principal Member of Technical Staff. In 2010, he returned to MIT as an Associate Professor.

His research focuses on photonic microsystems for low-power communications, sensing, and microwave-photonics applications. He has more than 100 authored or coauthored publications and more than a dozen issued patents. His current research interests include the modeling, fabrication, and the testing of large-scale implementations of microphotonic circuits, systems, and networks that are being integrated, directly or through hybrid techniques, with CMOS electronics for high-speed transmitting, switching, and routing applications of digital signals. Additional interests include large-scale microphotonic sensing and imaging arrays, along with optical phased arrays, nanophotonic antennas, nonlinear optics, and manipulations of optical-electromagnetic fields on-chip.

Dr. Watts is a member of the Optical Society of America (OSA).