An Ultra Low Power 3D Integrated Intra-Chip Silicon Electronic-Photonic Link

Erman Timurdogan[1], Zhan Su[1], Krishna Settaluri[2], Sen Lin[2], Sajjad Moazeni[2], Chen Sun[2], Gerald Leake[3], Douglas D. Coolbaugh[3], Benjamin R. Moss[1], Michele Moresco[1], Vladimir Stojanović[2], Michael R. Watts[1]

[1]Research Laboratory of Electronics, Massachusetts Institute of Technology, 77 Massachusetts Avenue, Cambridge, Massachusetts 02139, USA
[2]Berkeley Wireless Research Center, University of California, Berkeley, 2108 Allston Way, Suite 200, Berkeley, CA 94704 USA
[3]College of Nanoscale Science & Engineering, University at Albany, 1400 Washington Avenue, Albany, New York 12222, USA
ermant@mit.edu

Abstract: A record low energy (250fJ/bit) intra-chip electronic-photonic link is demonstrated at 5Gb/s on a 3D-integrated wafer using through-oxide-vias (1.45fF-per-via) for the first time. The receiver sensitivity was -19.3dBm and the on-chip laser energy was 6fJ/bit.

OCIS codes: (250.3140) Integrated optoelectronic circuits; (130.4110) Modulators; (040.5160) Photodetectors

1. Introduction

Computation within complementary-metal-oxide-semiconductor (CMOS) chips is doubling every eighteen months at a fixed energy budget and cost, following Moore's Law. This energy-constrained scaling is realized through the increasing use of multi-core architectures and the reduction of the switching power at progressive CMOS nodes. However, introducing multiple cores massively scales communication bandwidth and energy consumption within the chip. In fact, in emerging CMOS nodes, the communication power is expected to engulf the power budget for computations. On-chip electrical pipelined (repeated) links typically consume 50-to-100fJ/bit-per-mm (Figure 1-a) [1,2]. By 2020, a chip is expected to communicate at 576Tera-bits/sec over an average distance of one millimeter, consuming 58 Watts [1], almost equivalent to the power budget of a current chip including both communications and computations. Disruptive on-chip communication alternatives that reduce the energy-per-millimeter are required, leaving the majority of the power budget for computations. With the advent of low loss waveguides, optical communications are the ideal alternative for extending Moore's Law for both on-chip computations and communications. Among the integrated electronic-photonic platforms, silicon photonics is the only one that leverages existing CMOS-compatible fabrication, resulting in an insignificant cost penalty. On this platform, high speed and low power modulators (1fJ/bit at 25Gb/s [3]) as well as high bandwidth and high responsivity photodetectors [4] are already demonstrated. However, these benefits cannot be realized without close integration of silicon photonics to the CMOS electronics. The 3D integrated silicon photonics and electronics platform simultaneously enables close integration and independent optimization of each platform. However, existing 3D integrated electronics and photonics platforms are bottlenecked by the large parasitic capacitance (>30fF-per-via) of the interface (e.g. microbumps [5] or Through-Silicon-Vias (TSV) [6]).
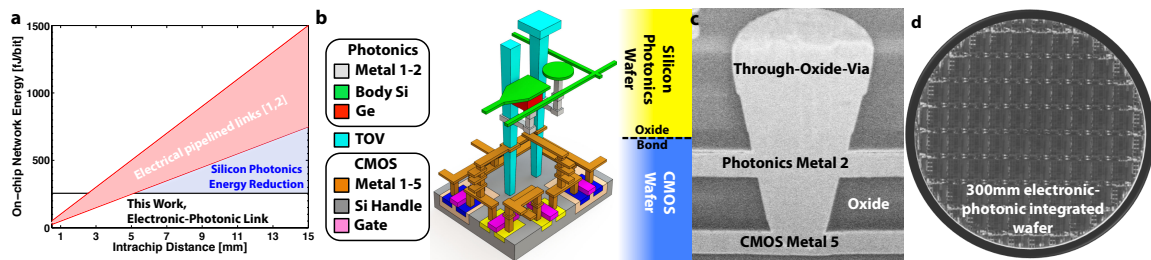

Figure 1, a) On-chip communication energy of the electrical and electronic-photonic intrachip link in a modern chip as a function of length. b-d) The 3D depiction and images of flip-wafer integrated silicon electronic-photonic 300mm platform with low capacitance interface (TOVs)

Here, we demonstrate for the first time a wafer-scale 3D electronic-photonic integrated platform, interfaced by the low capacitance (1.45fF-per-via) Through-Oxide-Vias (TOV) (Figure 1-b-d). The order-of-magnitude lower interface capacitance enabled this platform to realize a silicon electronics and photonics intrachip link that operated "error-free" (bit-error-rate < 10^{-12}) at 5Gb/s with a record low energy consumption of 250fJ/bit without signal equlization. When the data is fed directly into the integrated modulator driver, the integrated vertical p-n junction silicon microdisk modulator operated "error-free" at 12Gb/s. The integrated transmitter, consisting of the driver and the modulator, consumed only 9.4fJ/bit. The sensitivity of Ge detector-based integrated receiver was -19.2dBm at 5Gb/s, enabled by the high responsivity of 0.85A/W at λ~1510nm and low device capacitance of 7.55fF. Given this high sensitivity detector and low waveguide losses, the intra-chip link required an on-chip laser power of only -

15.2dBm or 6fJ/bit at 5Gb/s. These fixed costs indicate that optical link becomes more beneficial for lengths of more than 3mm, shown in Figure 1-a.

The silicon photonics was fabricated on a 300mm (silicon-on-insulator) SOI wafer with 100nm minimum feature size. A 65nm bulk CMOS electronics was also fabricated on a 300mm electronic wafer separately. The 300mm photonic wafer is flipped upside down to form an oxide-to-oxide bond between photonics and electronics. After bonding, the silicon handle is stripped off from the photonic SOI wafer. TOVs are drilled through the oxide to connect electronics and photonics top metal layers. Back metal is patterned only on top of the wirebonded TOVs, thereby eliminating excess capacitance (Figure 1-b,c).
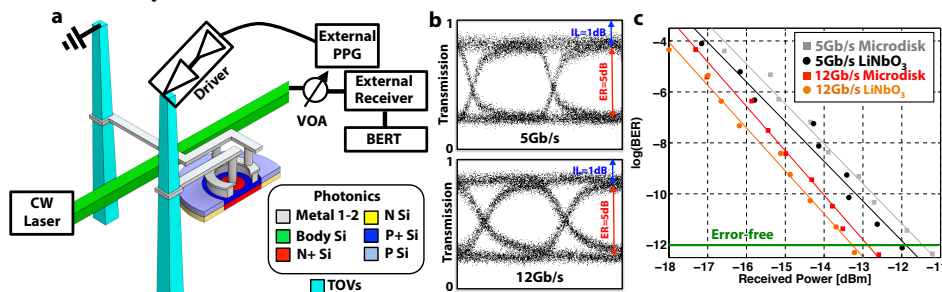
2. Measurements and Analysis

Figure 2, a) The 3D depiction of the integrated transmitter, including a modulator driver and the vertical junction microdisk modulator (cut to show the crossection). b) The open eye diagrams (extinction ratio (ER), insertion loss (IL)) at 5Gb/s and 12Gb/s for an NRZ-OOK PRBS modulated data and a pattern length of 2^{31}-1. c) The BER as a function of received power for an external LiNb03 modulator and the integrated transmitter.

First, we characterized the transmitter consisting of a vertical junction microdisk modulator and an on-chip driver (Figure 2-a). The fabrication and the performance details of the stand-alone microdisk modulator are explained in [3]. For high-speed measurements, an external pulse pattern generator (PPG) is used to generate a non-return-to-zero (NRZ) on-off-keying (OOK) pseudo-random-binary-sequence (PRBS) with a pattern length of 2^{31}-1. The PRBS data and complementary data, AC coupled 1.0Vpp signals, are applied to the integrated electronics with a non-terminated high-speed Infinity probe through the back metal pads. The differential current-mode receiver converted the external PRBS data to CMOS data, which is then fed to the modulator driver (two inverters) and microdisk modulator, thereby encoding electrical bits to optical bits. The supply was 1.2V and the modulator was driven in depletion mode from 0V to -1.2V. The CW laser is aligned to the transverse-electric (TE) resonance of the modulator (λ~1529nm) and the optical transmission was received with an external PIN-TIA detector. The received optical eye diagrams with 5dB extinction ratio and 1dB insertion loss at 5Gb/s and 12Gb/s are shown in Figure 2-b. For quantifying the signal integrity, the received data is attached to the external bit-error-rate tester (BERT) and the power after the chip is controlled with a variable optical attenuator (VOA). The BERT curves of the integrated modulator at 5Gb/s and 12Gb/s, shown in Figure 2-c, is compared to an external commercial lithium niobate (LibNO$_3$) Mach-Zehnder modulator. The integrated modulator exhibited "error-free" operation at 5Gb/s and 12Gb/s and the power penalty of the integrated modulator was 0.5dB at both data rates. The capacitance of the components was extracted from the measured switching energy, utilizing the electronic-photonic circuit replicas at each stage of integration. The total switching energy (E_s=CV^2) was 37.2fJ/bit and the total energy-per-bit of the transmitter was 9.4fJ/bit (E_{bit}=$CV^2/4$). The driver was connected to the modulator with two TOVs, having a capacitance per via of 1.45fF. Further, the modulator and driver capacitances were measured to be 9.5fF and 13.6fF, respectively.
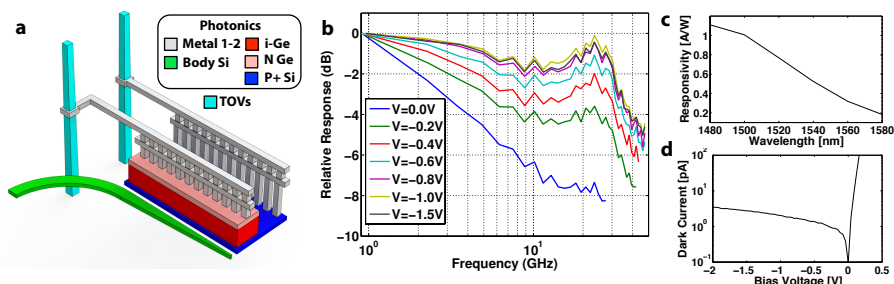

Figure 3, a) The 3D depiction of the Ge detector. b) The measured bandwidth as a function of applied reverse bias. c) The measured responsivity as a function of wavelength, >0.85A/W at λ~1510nm. d) The dark current as a function of bias voltage, 2.1nA or 52.5pA/μm^2 at -1V bias.

Second, we characterized a standalone Ge detector. The Ge is hetero-epitaxially grown into deep oxide trenches on top of body Si photonic layer. The coupling from the Si bus waveguide to Ge detector was achieved by an evanescent taper to the side of the detector, shown in Figure 3-a. The body Si layer under Ge is implanted by a p-

type dopant, details are explained in [2]. The body Si layer is extended to the side of the Ge to be contacted. The top layer of Ge is implanted by a shallow n-type dopant and contacted directly, forming a vertical p-i-n junction between the body silicon layer and the top of the Ge layer. The measured dark current density over the 300mm wafer was ranging from 50-to-90 $pA/\mu m^2$ at -1V reverse bias. A Ge detector, 4μm in width and 10um in length, is characterized and integrated with the receiver macro for the intrachip link below. The standalone detector had a 2.1nA dark current at -1V reverse bias (Figure 3-d) and the capacitance (C=εA/d) was only 7.55fF or $0.19fF/\mu m^2$. The bandwidth of the detector was measured using the heterodyne laser technique. The 3dB bandwidth, shown in Figure 3-b, was limited to 40GHz for detectors up to $40\mu m^2$, indicating transit time limited response rather than the RC time constant. The responsivity for TE mode is measured as a function of CW laser wavelength in Figure 3-c.
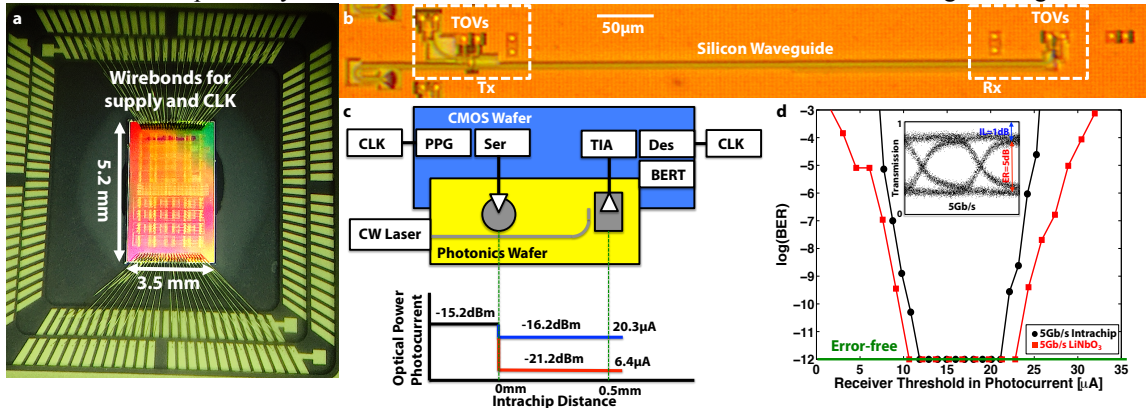

Figure 4, a-b) The 3D system chip and flip wafer integrated electronic-photonic intrachip link, involving functional photonic transmitter, recevier and TOVs. c) The sketch of the intrachip link with the optical power budget. d) The receiver BER curves of the intrachip link and a link formed with an external LiNbO₃ modulator.

Finally, we attached the standalone detector to the flip-wafer integrated receiver. The receiver consists of a TIA plus cascode pre-amplifier and a comparator. The transmitter macro, characterized above, is combined with the receiver to form a silicon electronic-photonic intrachip link within a system chip, shown in Figure 4-a,b,c. Within the system chip, there were 16-million functional transistors and over one thousand functional optical components and TOVs. To enable this large device count, the chip required a serializer and deserializer backend, which currently limits the bandwidth of the system chip to 5Gb/s. For characterizing the intrachip link in this platform, an NRZ-OOK PRBS data is seeded by an on-chip pattern generator (PPG) with a pattern length of 2^{31}-1. The data is fed to the driver/modulator, imprinting it onto the optical domain. A CW laser is aligned to the resonance of the modulator at λ ~ 1510nm. The input laser power was −15.2dBm. The insertion loss of the modulator was 1dB, the NRZ-OOK PRBS format introduced an additional ~3dB loss and waveguide loss was 1.4dB/cm. The received power at the detector, biased at -1.2V, was -19.2dBm and the average photocurrent was 13.3μA. An on-chip BERT circuit is used to quantify signal integrity of this link. The intrachip link transmitted and received bits with a BER <$1e^{-12}$ at a receiver threshold of 11.5μA, shown in Figure 4-b. When the integrated modulator is bypassed and the on-chip receiver is formed a link with an external commercial lithium niobate (LibNO₃) Mach-Zehnder modulator, the "error-free" receiver threshold was 10μA, indicating an intrachip link power penalty of only 0.5dB (same as modulator power penalty).

The energy consumption of this 5Gb/s link was a record low 250fJ/bit, where transmitter electronics and photonics consumed 9.4fJ/bit, receiver electronics consumed 240fJ/bit and the required input laser energy to achieve error-free operation was 6fJ/bit at 5Gb/s (-15.2dBm).

3. Conclusions

We demonstrated a flip-wafer integrated silicon electronic-photonic platform with low capacitance TOVs for the first time. The platform enabled an electronic-photonic intrachip link that consumed less energy than an electrical pipelined intrachip link. This is the first major step towards Moore's Law for on-chip communications, enabling fixed cost/energy at an increased bandwidth. Combined with the wavelength division and polarization multiplexing, the bandwidth of the photonic system can be readily scaled further.

4. References

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