

# High-density 3D Electronic-Photonic Integration

V. Stojanović<sup>1</sup>, K.T. Settaluri<sup>1</sup>, S. Lin<sup>1</sup>, S. Moazeni<sup>1</sup>, E. Timurdogan<sup>2</sup>, C. Sun<sup>1</sup>, M. Moresco<sup>2</sup>, Z. Su<sup>2</sup>, Y-H. Chen<sup>2</sup>, G. Leake<sup>3</sup>, D. LaTulipe<sup>3</sup>, C. McDonough<sup>3</sup>, J. Hebding<sup>3</sup>, D. Coolbaugh<sup>3</sup>, M. Watts<sup>2</sup>

<sup>1</sup>University of California, Berkeley

<sup>2</sup>Massachusetts Institute of Technology

<sup>3</sup>College of Nanoscale Science and Engineering SUNY Polytechnic Institute

Today's electronic photonic integration approaches involve various trade-offs between integration complexity, cost and performance, with no single approach being able to satisfy both the high-performance and low cost/complexity requirements. Luxtera's process [1] represents monolithic integration, which has low parasitics and customized photonics but slow transistors. Oracle's [2] and ST Micro [3] integrate photonic chips and electronic chips through face-to-face micro-bump/copper-pillar bonding, which enables fast transistors, optimized photonics but at the cost of high interconnection parasitics (both electrical wirebond to the outside world and chip-to-chip bumps) which limit the link performance. Another monolithic approach recently demonstrated monolithic integration of photonic components in an advanced process node (45nm SOI) [4] and offers the promise of high-speed transistors, low-parasitics, but somewhat constrained photonic devices. In this paper, we illustrate an alternative approach that we recently demonstrated, which aims to offer the best of both worlds by performing 3D integration of electronic and photonic wafers with very low interconnection parasitics. In Figure 1, we illustrate the process in which the photonic SOI wafer is oxide bonded face-to-face with the CMOS wafer (shown on the bottom). The substrate of the photonic wafer is then removed and connections between the CMOS wafer and the photonic wafer are established through tight-pitch shallow (depth less than 7 $\mu$ m) through-oxide vias (TOVs). The parasitic capacitance of the TOV is estimated to be around 3fF from on-chip de-embedding structures. This is critical to improved energy efficiency of the transmitter and receiver sensitivity to optical power. In comparison, the capacitance of the micro-bump/copper-pillar connection is at least 10x larger. Figure 2 illustrates one of the chip templates in this electronic-photonic development platform. This chip template hosts 16 complete photonic transceiver modules, each implemented to enable up to 8 different modulators and photo-detectors to be tested with the same electronic back-end, to aid in process characterization and device development. Each front-end in this multi-cell macro consists of the modulator driver with serializer and thermal-tuning lock circuitry, a receiver with deserializer and thermal lock circuitry and a common digital back-end for data-generation, link performance monitoring and configuration. This development platform template yields 1000s of functional photonic components as well as 16M transistors per chip module. Figure 3 illustrates a full optical chip-to-chip link is demonstration. The transmitter operates at 6Gb/s with an energy cost of 100fJ/bit and the receiver at 7Gb/s with a sensitivity of 26 $\mu$ A (-14.5dBm) and 340fJ/bit energy consumption. A full 5Gb/s chip-to-chip link, with the on-chip calibration and self-test, is demonstrated over a 100m single mode optical fiber with 560fJ/bit of electrical and 4.2pJ/bit of optical energy.

Acknowledgment:

This work was supported by the Defense Advanced Research Projects Agency (DARPA) of the United States under the E-PHI project, grant no. HR0011-12-2-0007 and DARPA MTO Program Manager Dr. Josh Conway and also in part by W911NF-12-1-0210 under Dr. Jag Shah.

References:

- [1] Gunn, C., "CMOS Photonics for High-Speed Interconnects," in *Micro*, IEEE, vol.26, no.2, pp.58-66, March-April 2006.
- [2] F. Liu, *et al.*, "10-Gbps, 5.3-mW Optical Transmitter and Receiver Circuits in 40-nm CMOS," in *Solid-State Circuits, IEEE Journal of*, vol.47, no.9, pp.2049-2067, Sept. 2012
- [3] F. Boeuf, *et al.*, "Recent Progress in Silicon Photonics R&D and Manufacturing on 300mm Wafer Platform," in *Optical Fiber Communication Conference, OSA Technical Digest (online) (Optical Society of America, 2015)*, paper W3A.1.
- [4] C. Sun, *et al.*, "A 45nm SOI Monolithic Photonics Chip-to-Chip Link with Bit-Statistics-Based Resonant Microring Thermal Tuning," *IEEE Symposium on VLSI Circuits*, Kyoto, Japan, 2 pages, June 2015.
- [5] K.T. Settaluri, *et al.*, "Demonstration of an Optical Chip-to-Chip Link in a 3D Integrated Electronic-Photonic Platform," *European Solid-State Circuits Conference, Gratz, Austria*, 4 pages, September 2015.
- [6] E. Timurdogan, *et al.*, "An Ultra Low Power 3D Integrated Intra-Chip Silicon Electronic-Photonic Link," [Post-deadline] *Optical Fiber Communication Conference, Los Angeles, CA*, 3 pages, March 2015.

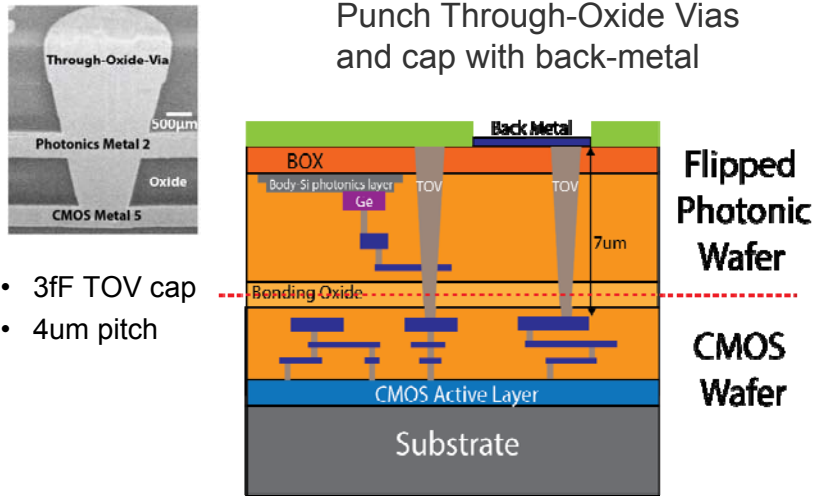


Figure 1. Electronic-Photonic 3D integration with Through-Oxide technology

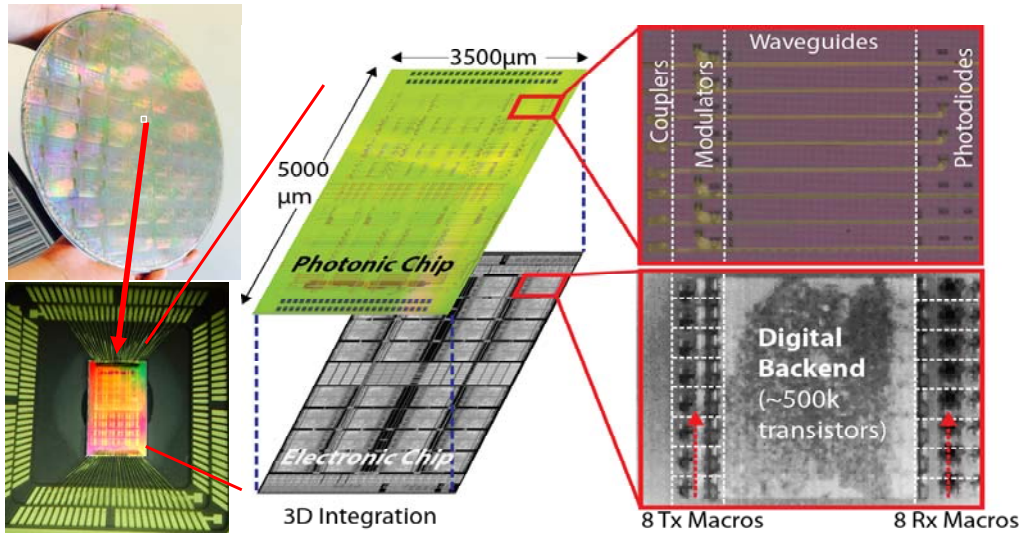


Figure 2. Electronic-Photonic 3D integration platform: photonic link multi-cell template

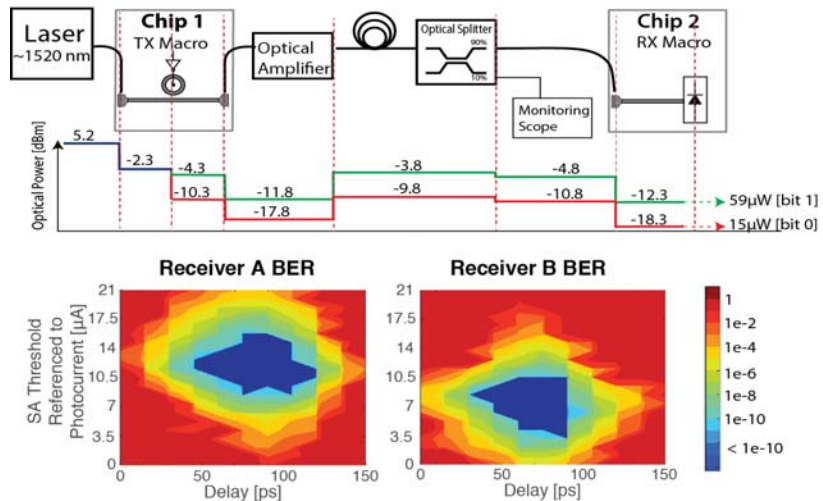


Figure 3. 3D Integrated chip-to-chip photonic link result at 5Gb/s