Demonstration of an Optical Chip-to-Chip Link in a 3D Integrated Electronic-Photonic Platform

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***Abstract*—A full optical chip-to-chip link is demonstrated for the first time in a wafer-scale heterogeneous platform, where the photonics and CMOS chips are 3D integrated using wafer bonding and low-parasitic capacitance thru-oxide vias (TOVs). This development platform yields 1000s of functional photonic components as well as 16M transistors per chip module. The transmitter operates at 6Gb/s with an energy cost of 100fJ/bit and the receiver at 7Gb/s with a sensitivity of 26μA (-14.5dBm) and 340fJ/bit energy consumption. A full 5Gb/s chip-to-chip link, with the on-chip calibration and self-test, is demonstrated over a 100m single mode optical fiber with 560fJ/bit of electrical and 4.2pJ/bit of optical energy.**

Keywords—optics; link; heterogeneous; 3D integration; transceivers;

I. Introduction

Silicon photonics has stepped up as a clear contender in enhancing the capabilities of CMOS applications through lower energy and higher bandwidth density over traditional electrical I/O. Additionally, optical links benefit from distance insensitivity due to the inherently low loss of fibers, allowing for new types of connectivity and network organization in modern digital systems and data-centers. Wavelength-division multiplexing (WDM) may also be realized to place many data channels on a single optical fiber, thereby increasing the bandwidth density while retaining energy efficiency and breaking the I/O pin limitations imposed by the electronics.

To enable full optical links for interconnection networks, high speed and low power optical transmitters as well as high bandwidth and high sensitivity optical receivers are required. These necessitate the need for close integration in order to achieve small parasitic capacitance between electronics and photonic devices. Furthermore, a two-wafer solution is desirable to separately optimize the performance of the photonic components and the CMOS circuits.

This paper demonstrates for the first time an optical chip-to-chip link built in a heterogeneous, 3D integration platform using thru-oxide via (TOV) technology [1,2]. The TOV technology overcomes the challenges of close integration of electronic and photonic components, by simultaneously enabling separate wafer optimization of electronic and photonic components while providing a low-capacitance, high-density connection between the photonic and electronic wafers.

II. 3D Integration of CMOS and Photonics

Traditional heterogeneous platforms capitalize on the ability to individually optimize the photonic and electronic macros, an element missing in other forms of integration. However, the large interface capacitance associated with thru-silicon via (TSV) and μ-bump technologies limits the overall system performance as well as energy-efficiency.

As illustrated in Fig. 1, in this process, 300mm photonic and electronic wafers are manufactured separately in CNSE 300mm foundry and then bonded face-to-face using oxide bonding. The silicon substrate is then removed on the photonic SOI wafer and TOVs are punched through at 4μm pitch to connect the top layer metal of the photonic wafer to the top layer metal on the 65nm bulk CMOS wafer.

For packaging, wire-bonded back metal pads are deposited on top of the selected TOVs. The connection from the CMOS wafer to the photonic device is achieved through the TOVs passivated on top with an oxide layer, which minimizes the parasitic capacitance. Our measurements estimate the TOV capacitance to be ~3fF, which enables low-power and high-sensitivity electronic-photonic systems for a variety of applications. This represents an *order of magnitude* reduction in parasitic capacitance, and *two orders of magnitude* higher density compared to previously demonstrated μ-bump flip-chip electronic-photonic integration [3].

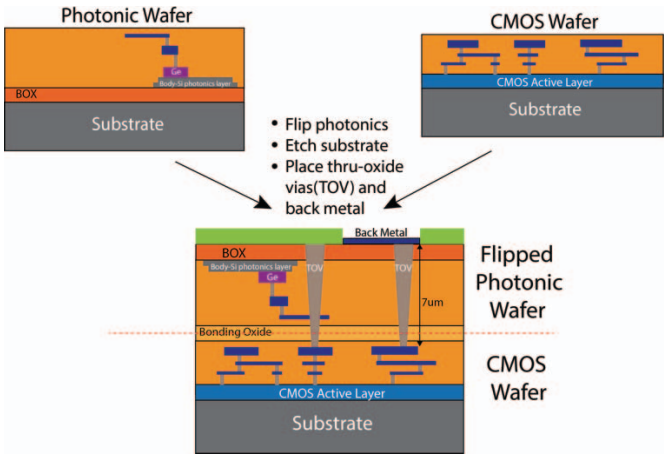

Fig. 1. Cross-section of 3D TOV hetrogeneous integration process

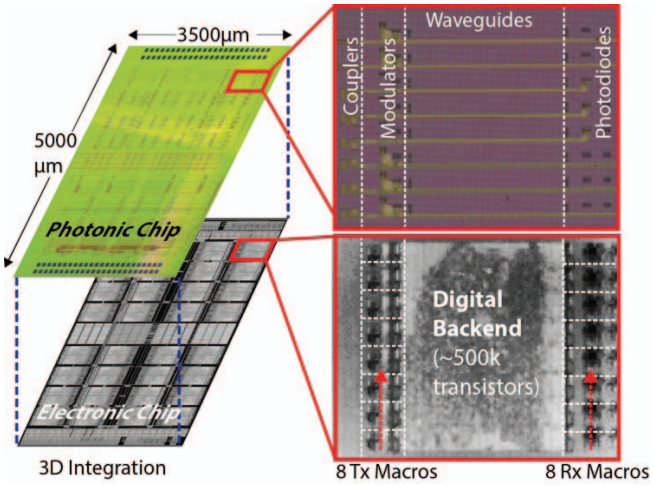

Fig. 2. Photonic and CMOS die views and Multicell architecture

III. Chip Architecture

The optical chip-to-chip link is a part of the wafer-scale heterogeneously integrated technology-development and demonstration platform with low-energy optical transmitters, receivers, and comprehensive backends for performance characterization (Fig. 2). Apart from containing vertical junction depletion mode microdisk modulators [4] within the photonics die, hetero-epitaxially grown Germanium photodiodes and body crystalline silicon low-loss waveguides are also used to enable electro-optic transceiver functionality. The 16M transistor electronic chip contains 32 *Multicell* sub-blocks that enable a full self-test of modulators and receivers within the link. Each *Multicell* is composed of eight RX as well as eight TX macros, enabling in-situ testing of a wide variety of photonic devices. The *Multicell* also contains an expansive digital backend infrastructure to enable full, self-contained characterization of each of the eight TX and RX sites. Characterization is accomplished through on-chip, self-seeding PRBS generators and counters. The 2^{31}-1 length PRBS data sequence gets fed into one of the TX macro sites, which serializes the data and drives the resonant modulator device imprinting the data sequence on the light in photonic waveguide. On the RX side, this modulated light is fed into one of the eight RX macros. The output of this RX macro is an eight-channel bus, marking the deserialized input optical data. These eight channels proceed on into the backend's bit-error-rate (BER) checkers, which count the total number of errors between the received data from the RX macro and the ideal sequence provided by the seeded PRBS generator.

A. Transmitter Design

The TX macro (Fig. 3) consists of a tunable vertical junction depletion-mode ring resonator similar to [2, 4] driven by an 8-to-1 serializer and driver head with on-chip PRBS input. The applied reverse-bias voltage to the junction via the driver head depletes free carriers and perturbs the refractive index of silicon, which in turn shifts the resonance wavelength (or frequency) of the optical modulator. The cathode of the modulator diode is connected to 1.2V while the anode is modulated from 0 to 1.2V. The modulator p-n junction is reverse-biased during modulation.

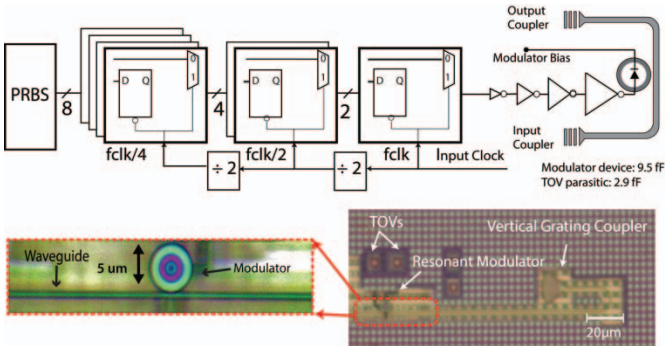

Fig. 3. Transmitter schematic and die photos

Given that the leakage current is small, the energy is consumed only when the transitions charge the reverse-biased junction capacitor. With a total modulator driver capacitive load of 12.4fF (modulator diode and TOV), at 6Gb/s the whole macro consumes 100fJ/b (5fJ/b modulator, 15fJ/b driver, and 80fJ/b serializer).

Heterogeneous integration allows us to use the state-of-the-art ring resonant modulators with a large electro-optic response of 150pm/V (20GHz/V), which enables low power modulation using small voltage swing (1.2V) while still maintaining sufficient extinction ratio (Fig. 4(a)). Measured from the modulator transmission spectra at 0V and -1.2V dc biases, the device should ideally achieve 6.2dB extinction ratio (ER) and 1.8dB insertion losses (IL). The modulator can also be modulated between a slightly forward-biased regime and depletion regime by lowering the bias voltage of the anode (i.e. -0.2 to 1.0V). This will further improve extinction ratio of the modulator.

A tunable CW laser source was coupled to an on-chip silicon waveguide through a vertical grating coupler. The laser frequency was aligned adjacent to the resonance frequency of the modulator ring (λ ~1520nm, see Fig. 4(a)). The TX circuits drive the 31-bit PRBS sequence into the modulator, achieving the non-return to zero on-off keying (NRZ-OOK) modulation eye at 6Gb/s, as shown in Fig. 4(b), with 6dB extinction ratio and 2dB of insertion loss, which agrees well with the transmission spectrum. The fast rise-time indicates the potential for faster operation, but the results are currently limited by the global high-speed clock distribution network that spans the whole chiplet and supplies the clock to all the *Multicell* macros.

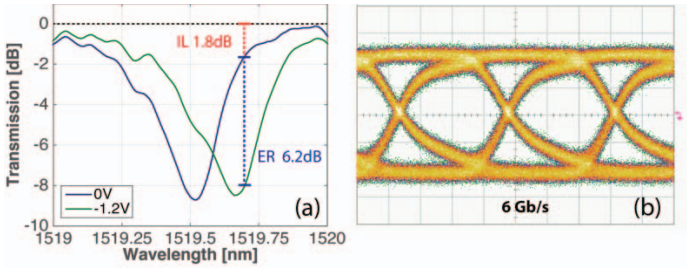

Fig. 4. Measured modulator transmission spectrum and eye diagram

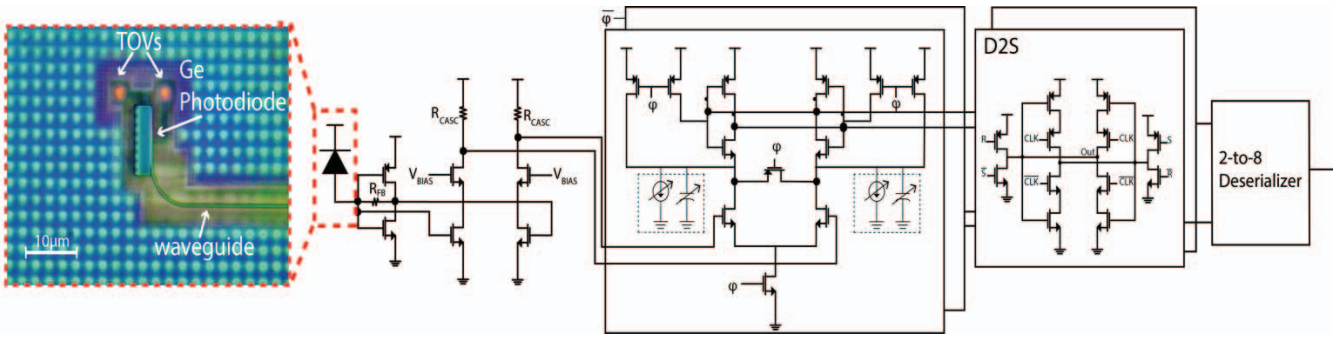

Fig. 5. Receiver architecture and photodiode die photo

B. Receiver Design

The receiver (Fig. 5) consists of a Ge photodiode placed on top of the electronics and connected to the receiver circuitry via TOVs with minimal parasitic capacitance. The TIA-based receiver circuit has a pseudo-differential front-end with a cascode pre-amplifier feeding into double-data rate (DDR) sense-amplifiers and dynamic-to-static converters (D2S). The TIA stage with 3kOhm feedback contains a 5-bit current bleeder at the input node, which is set to the average current of the photodiode. This allows the TIA input and output to swing around the midpoint voltage of the inverter. The TIA input and output are directly fed into a cascode amplifier with resistive pull up.

The bias voltage of the cascode is tuned through a 5-bit DAC. Adjusting this bias voltage results in a trade-off between the output common-mode voltage and the signal gain of the cascode stage. More specifically, increasing this bias voltage results in a higher cascade gain but lower output common-mode voltage that reduces the sense-amplifier speed. For a given data rate, an optimal bias voltage is determined so as to minimize the overall evaluation time of the sense amplifier. The proceeding sense amplifiers then evaluate the cascode outputs before getting deserialized and fed into on-chip BER checkers. Each sense amplifier has a coarse, 3-bit current bleeding DAC as well as a fine, 5-bit capacitive DAC for offset correction. An external Mach-Zehnder modulator with extinction ratio of about 10dB driven by an FPGA-sourced PRBS sequence is coupled into the chip to enable stand-alone receiver characterization. During the initial seeding phase, the incoming receiver data are used to seed the on-chip PRBS generators for the BER check. The receiver and deserializer achieve 7Gb/s with a BER below 10^{-10}.

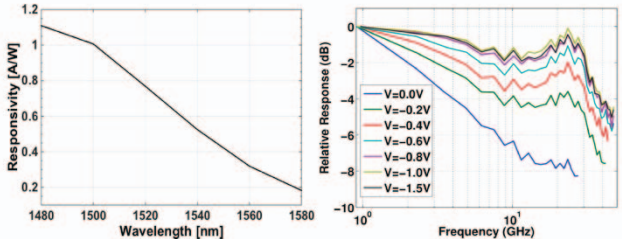

Fig. 6. Measured photodiode responsivity over 100 nm wavelength range and its frequency response (with 50Ohm load) for different bias voltages

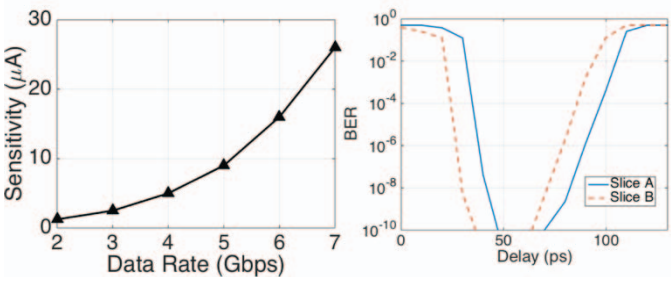

Fig. 7. Measured receiver average photo-current sensitivity over different data rates and BER bathtub curves for both receiver slices

The responsivity and bandwidth of this process variant of the Ge photodiode in [2], are shown in Fig. 6. At 1520nm, the responsivity is 0.73A/W, resulting in optical RX sensitivity of -14.5dBm at 7Gb/s, for electrical sensitivity of 26μA. The overall energy consumption is 340fJ/bit. The TIA+cascode pre-amplifier stage consumes 70fJ/bit. The sense amplifier, current plus capacitive correction DACs, and the dynamic-to-static converter together consume 120fJ/bit. Finally, the deserializer consumes 150fJ/bit. Figure 7 shows the sensitivity of the receiver as a function of data rate. Additionally, bathtub curves for the two slices of the DDR receiver are also shown.

IV. Link Implementation

A 100-meter optical link operating at 5Gb/s is demonstrated (Fig. 8) illustrating the functionality of all the required optical and electrical components in this heterogeneous platform. Figure 8 also shows the optical power breakdown per stage within the full link. A CW laser at λ~1520nm is coupled to the on-chip TX macro of Chip 1 using a vertical grating coupler. The coupler results in 7.5dB of loss in optical power. A PRBS generated data within this TX macro are fed into the modulator driver, which in turn modulates the ring resonator. The output of the TX macro including the coupler is the modulated light with 6dB extinction ratio. This light is fed into an optical amplifier providing 8dB of gain. The 8dB amplifier is necessary to mitigate part of the 15 dB chip-to-chip coupler loss in the optical data path (7.5dB per coupler) due to unoptimized coupler designs. The amplifier feeds into the 100 meter fiber proceeded by a 90/10 power splitter. A monitoring scope, using the 10% output, is used to ensure that an optical eye is visible. The 90% output is coupled into the RX macro. The Ge

photodiode is used within the RX macro to convert incoming optical data to an electrical bit stream. This photodiode sees -12.3dBm and -18.3dBm optical power for a bit 1 and 0, respectively. Figure 8 shows the output BER plot indicating at least 10^{-10} bit accuracy. This BER plot sweeps two parameters within the RX macro. First, the delay of the RX clock with respect to the TX clock is shown on the x-axis. Second, the corrective capacitor DAC within the receiver sense amplifiers is swept and shown on the y-axis. For particular delays and capacitive DAC values, a steady BER < 10^{-10} is observed, illustrating the margins for the robust operation of the link. The transceiver electrical energy cost is 560fJ/bit and the optical energy cost is 4.2pJ/bit (taking into account the amplifier gain). With optimized couplers (<3dB readily achievable in literature [6]), the required optical energy would scale down to below 0dBm (200fJ/bit) thereby eliminating the need for the optical amplifier.

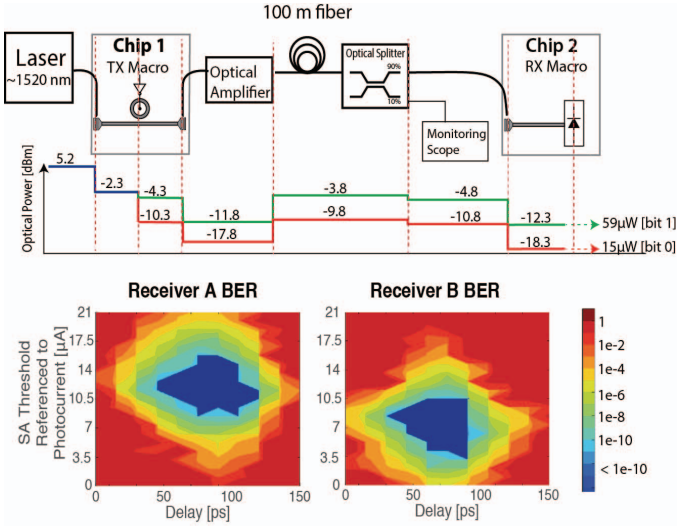

Fig. 8. Full optical link with optical power budget and performance

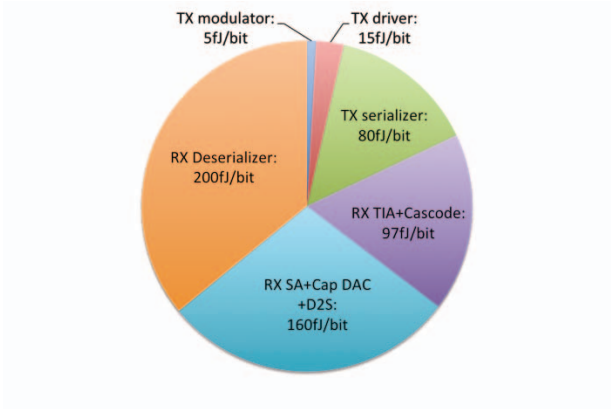

Fig. 9. Electrical energy breakdown for TX and RX macros in a 5Gb/s link

Figure 9 shows the electrical power breakdown of TX and RX macros within the link at 5Gb/s data rate. Table I presents the comparison to previous non-monolithic electronic-photonic transceiver works.

V. Conclusion

This work demonstrates the first large-scale 3D integrated photonic chip-to-chip link manufactured in a 300mm CMOS foundry. The functional 3D-assembled chips with 16M transistors and 1000s of photonic devices illustrate the high yield of the CMOS, photonic fabrication and 3D integration processes.

TABLE I. Comparison to previos works

	This work	**[3]**	**[5]**
CMOS Technology	65nm	40nm	65nm
Integration	Flip-Wafer 3D TOV	Flip-Chip µbump	Flip-Chip
RX Data rate [Gb/s]	7	10	8
RX Energy [fJ/b]	340	395	275
RX Area [mm^2]	0.0025	0.02	0.036
$C_{interconnect}$ [fF]	3	30	200
RX Ckt. Sens. [µA]	26	20	53.7
RX Opt. Sens. [dBm]	-14.5	-15	-12.7
TX Data rate [Gb/s]	6	10	5
TX Energy [fJ/b]	100	140	808
TX Area [mm^2]	0.0015	0.0012	0.04
Link DR [Gb/s]	5	10	-
Link Energy [fJ/b]	560	535	

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